

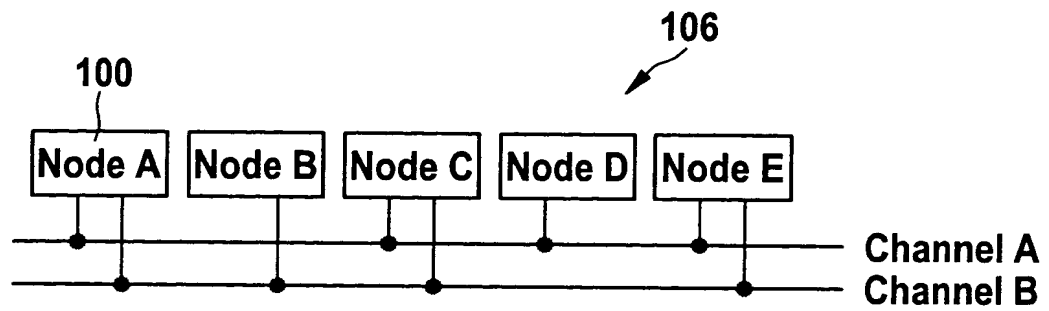
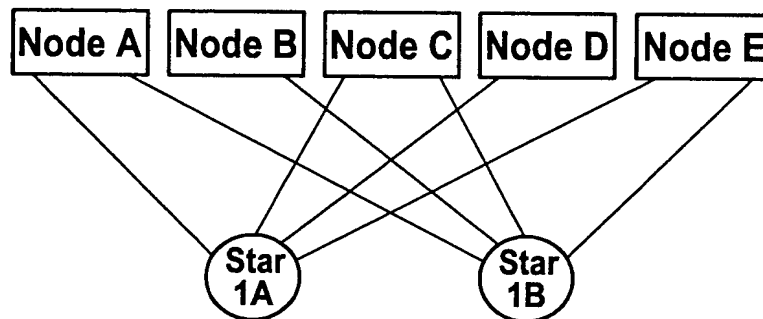
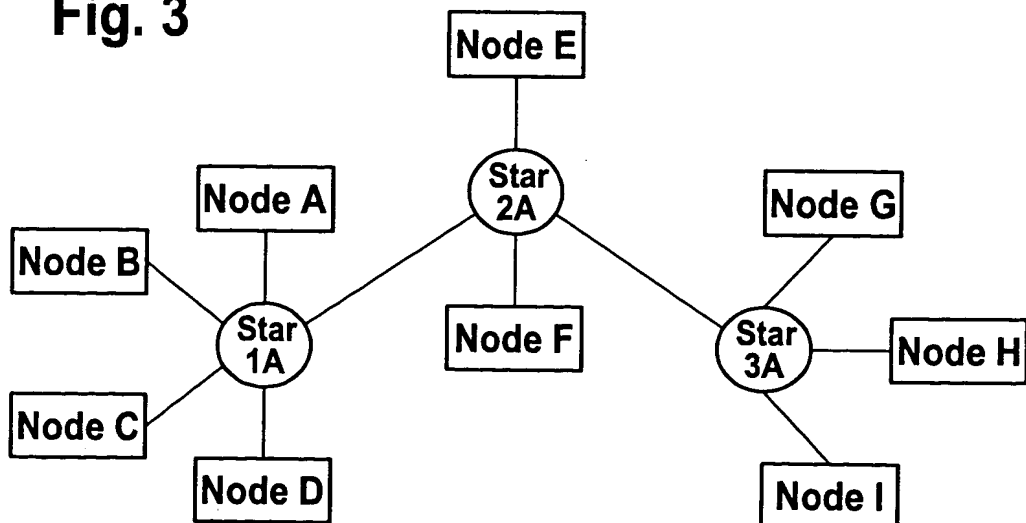
Fig. 1**Fig. 2****Fig. 3**

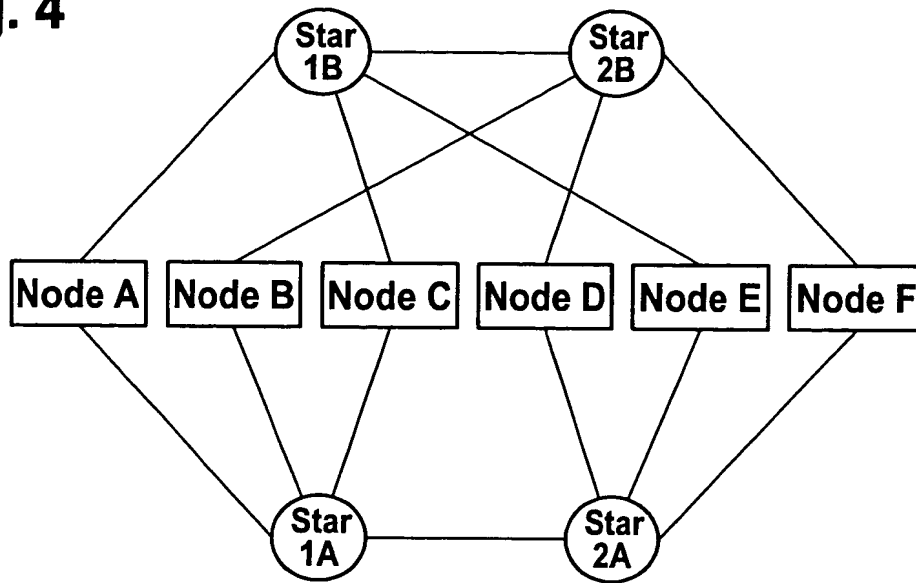
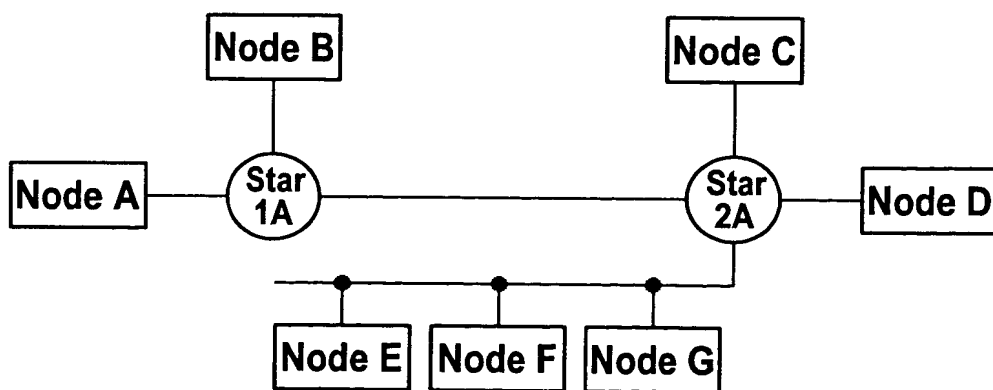
Fig. 4**Fig. 5**

Fig. 6

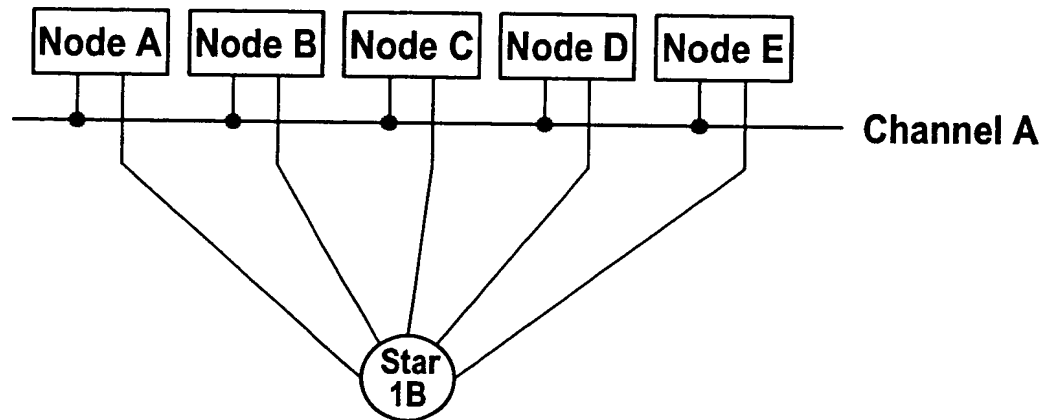


Fig. 7

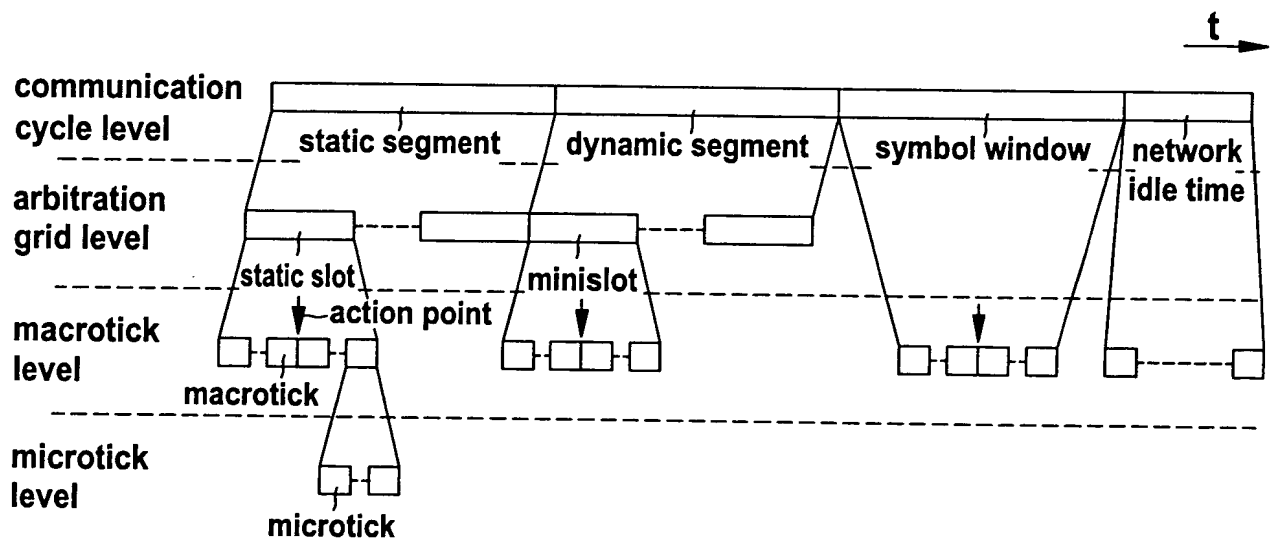


Fig. 8

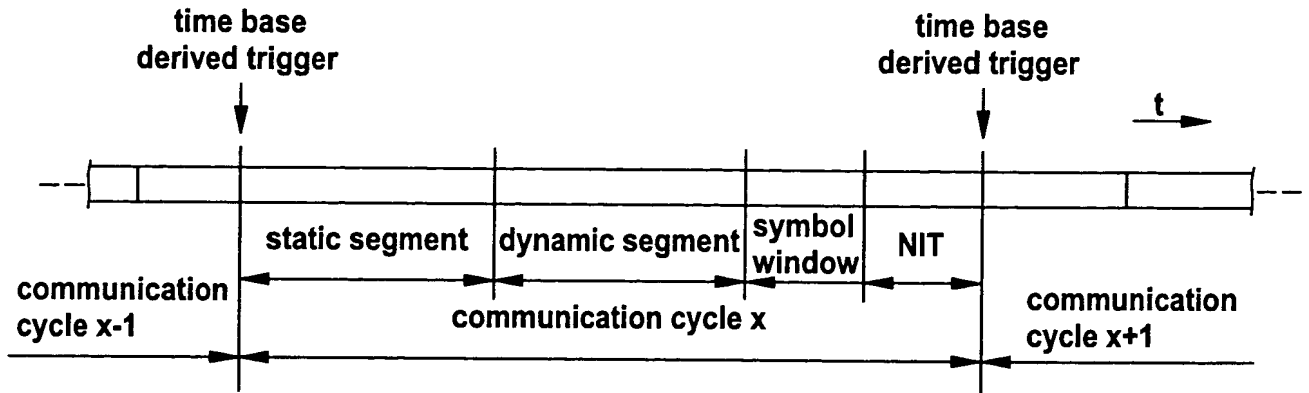


Fig. 9

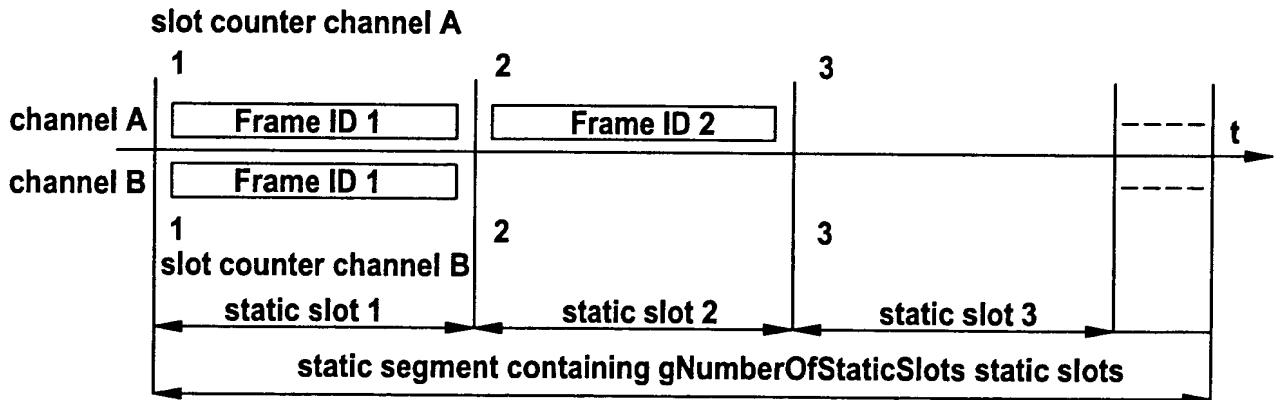


Fig. 10

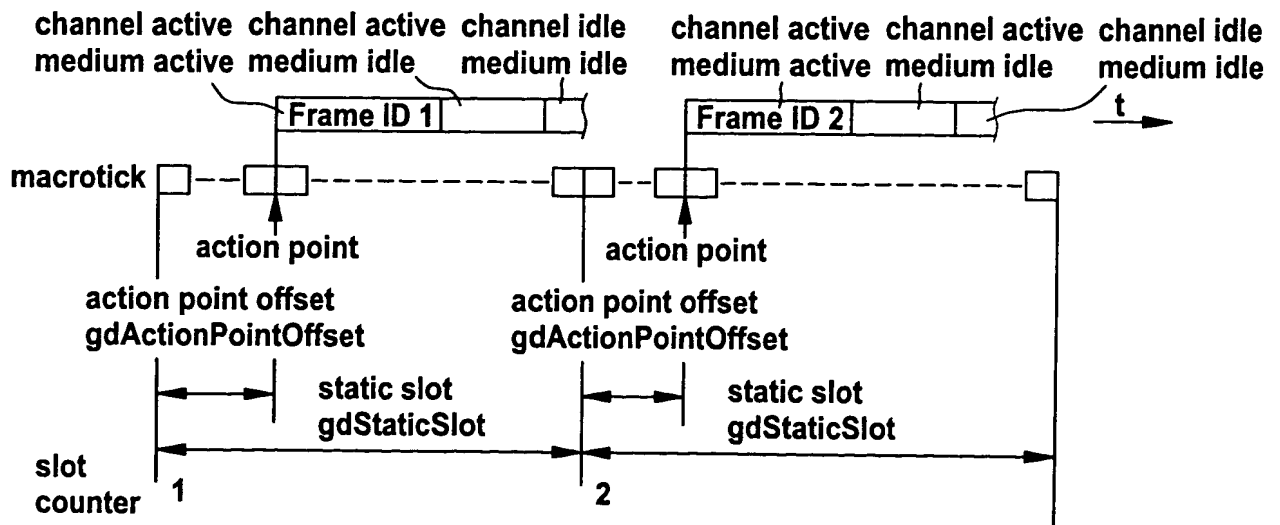


Fig. 11

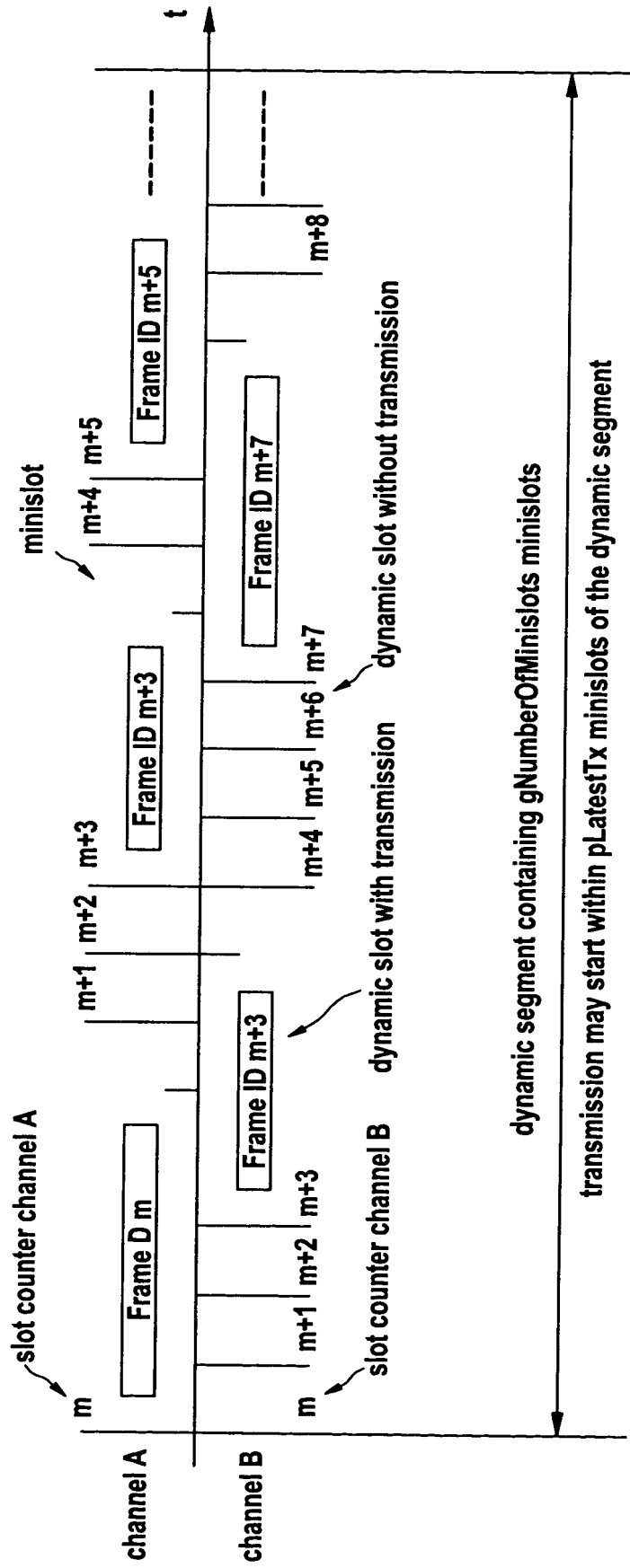


Fig. 12

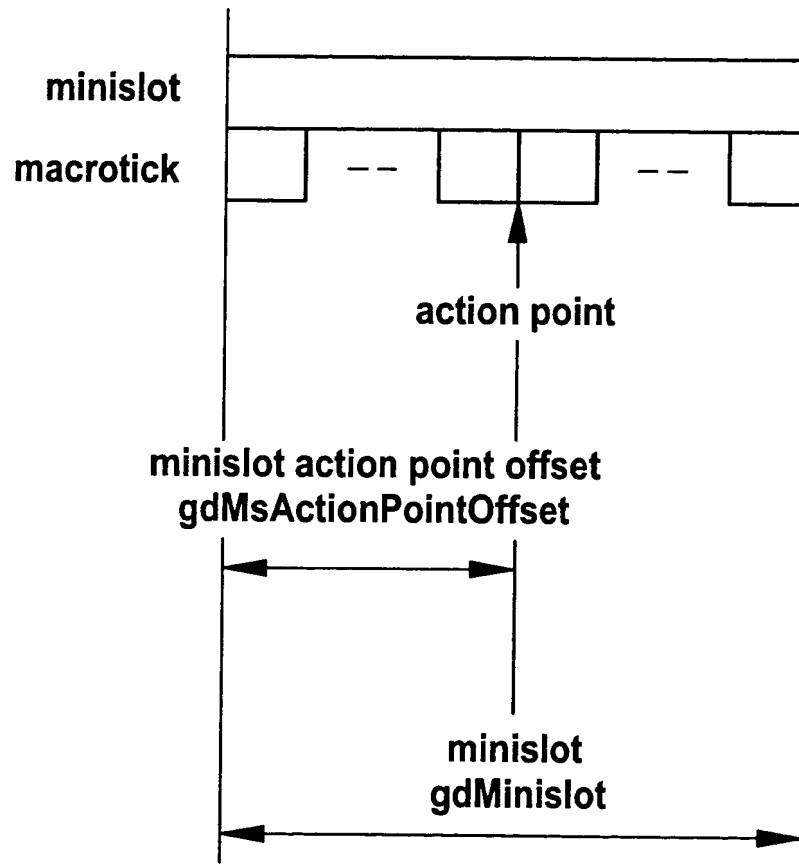


Fig. 13

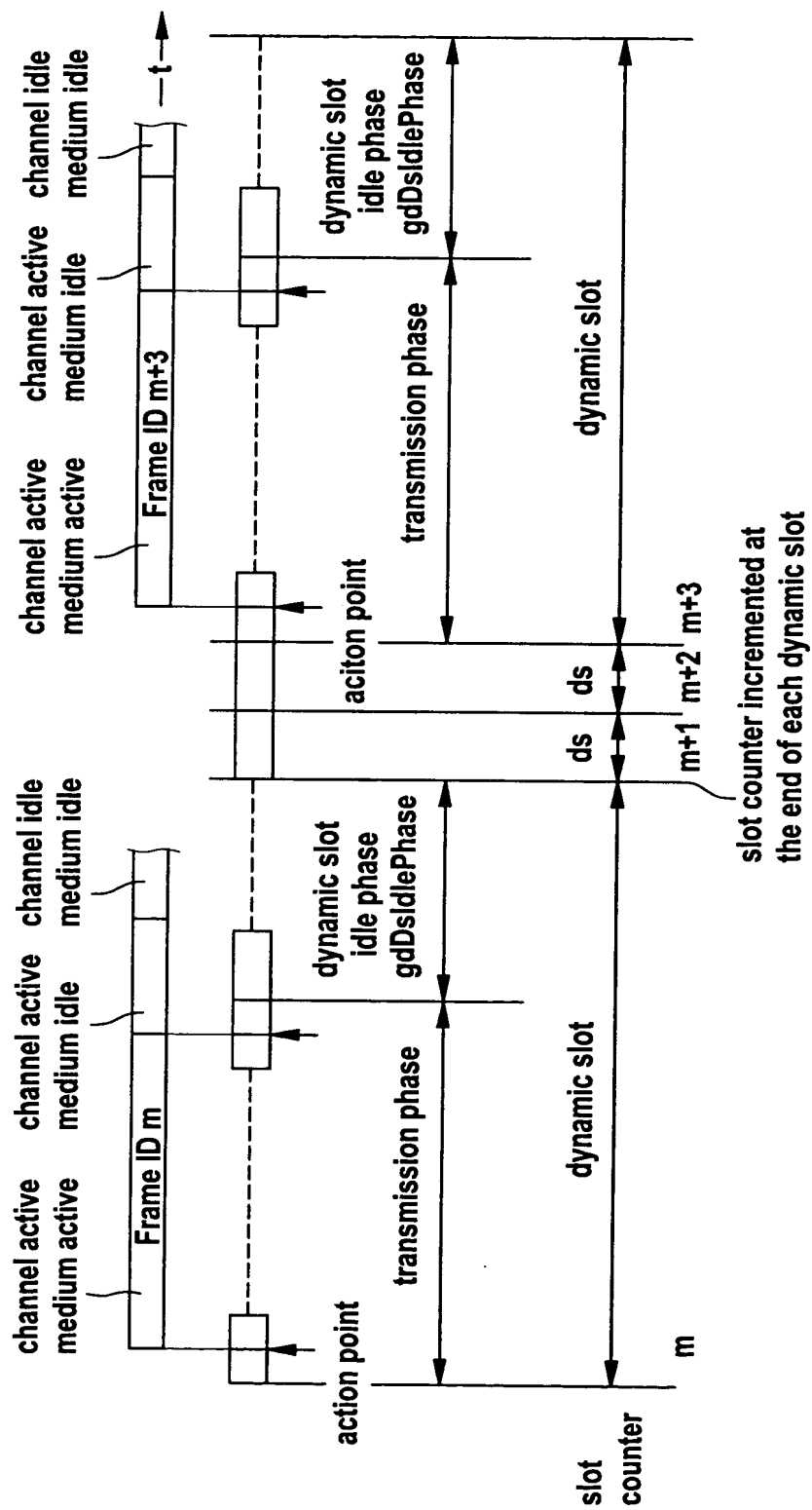


Fig. 14

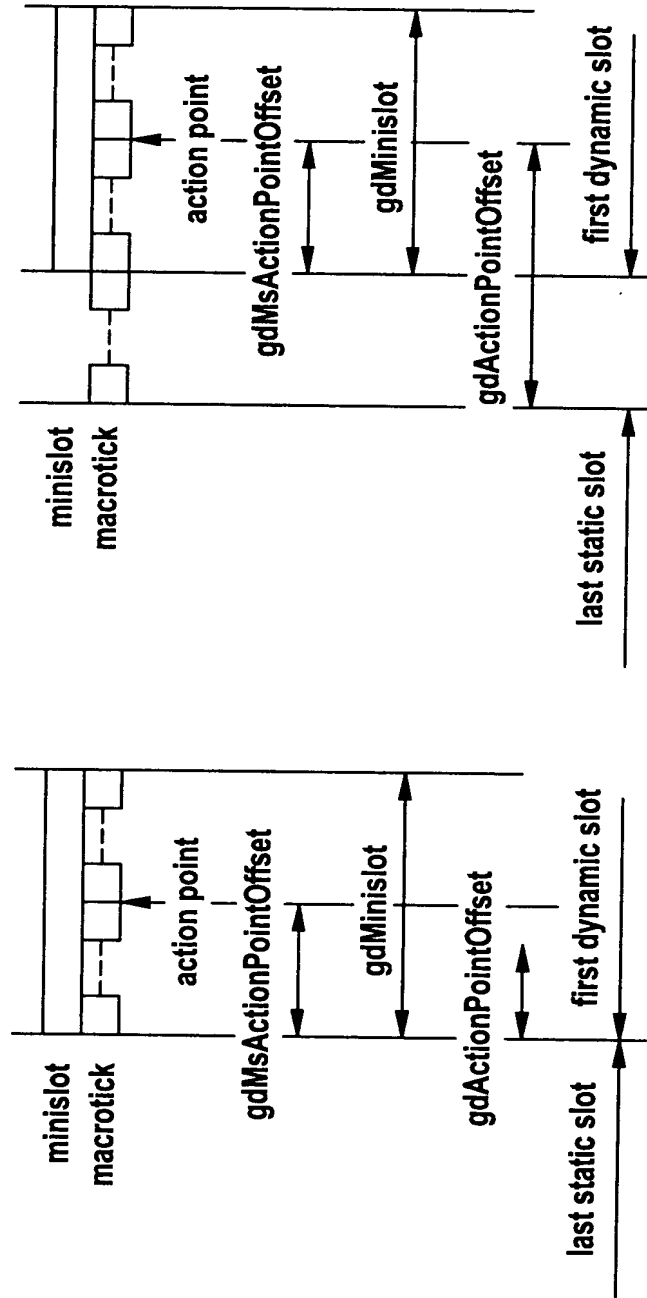


Fig. 15

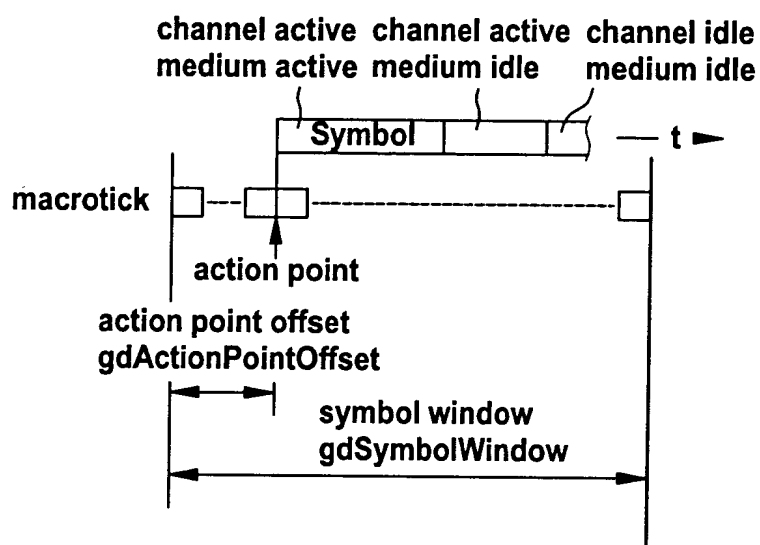


Fig. 16

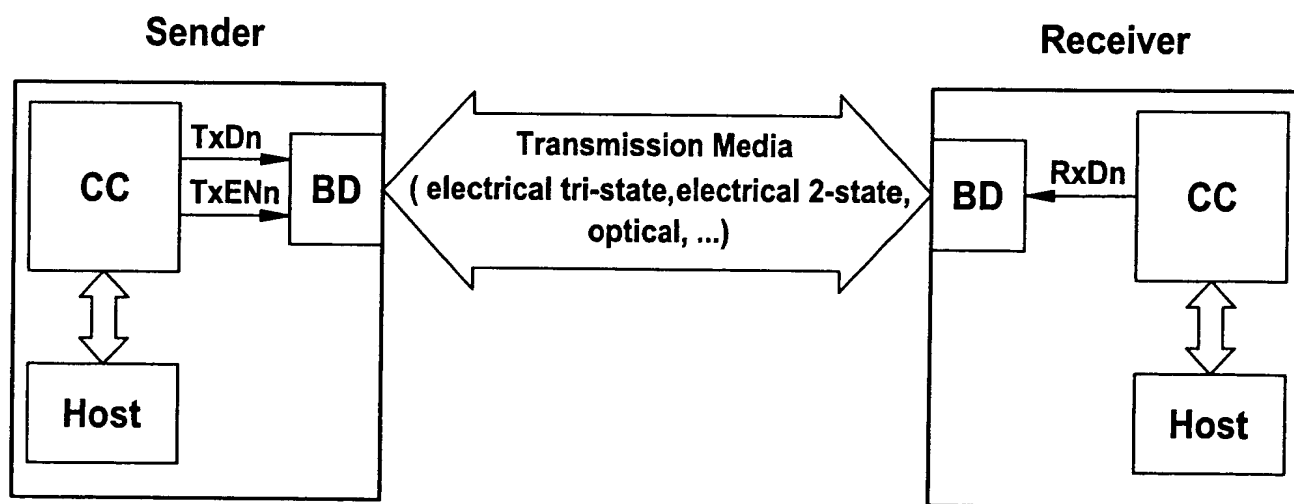


Fig. 17

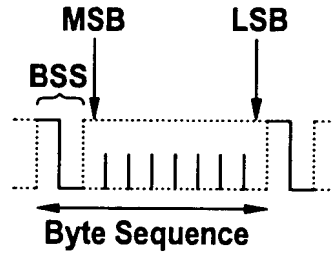


Fig. 18

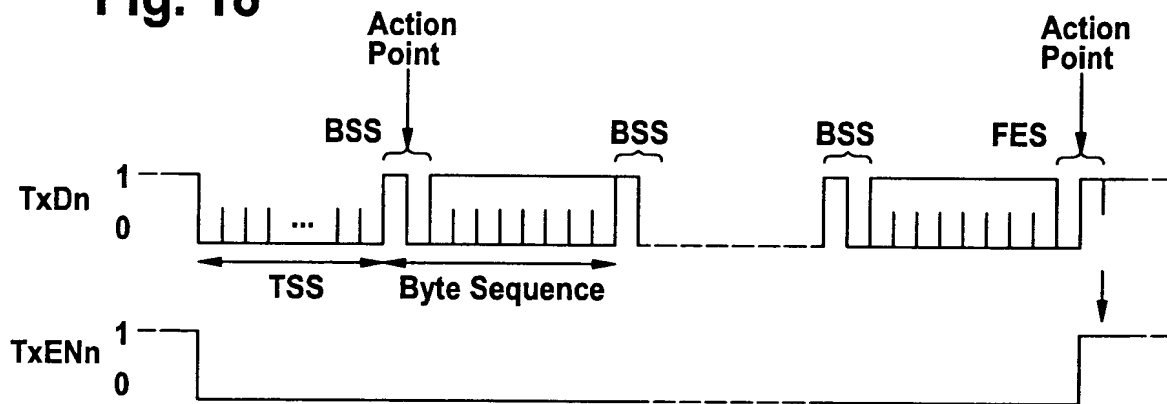


Fig. 19

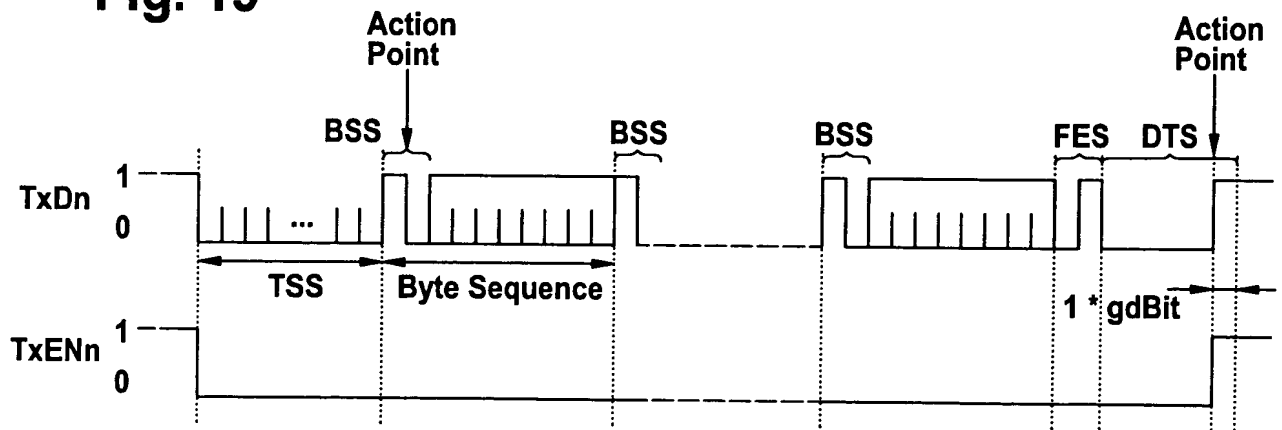


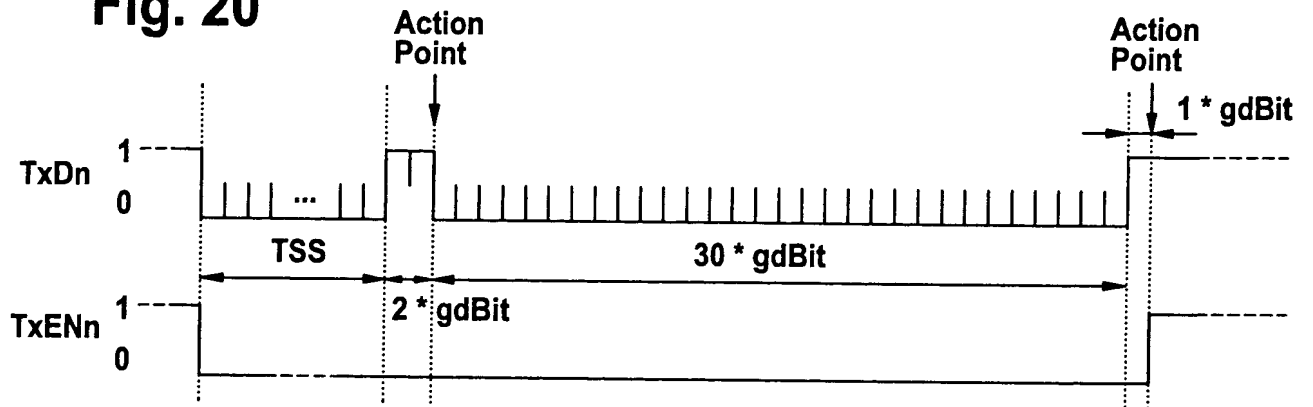
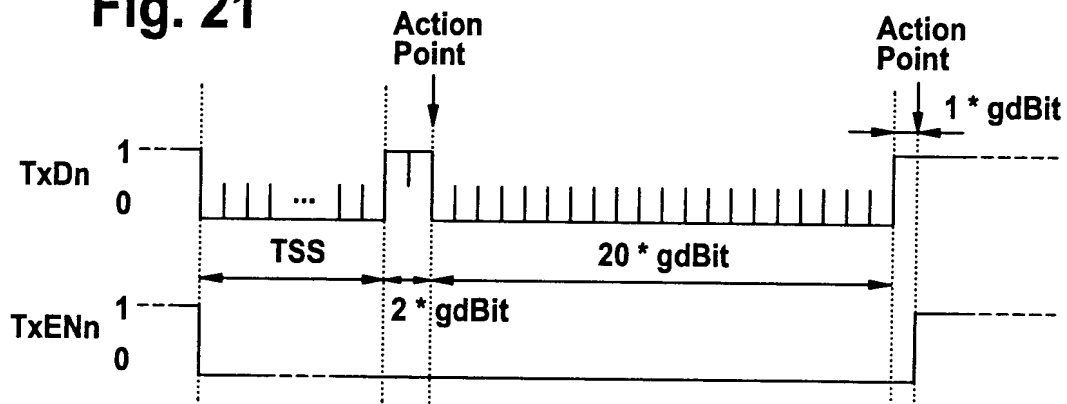
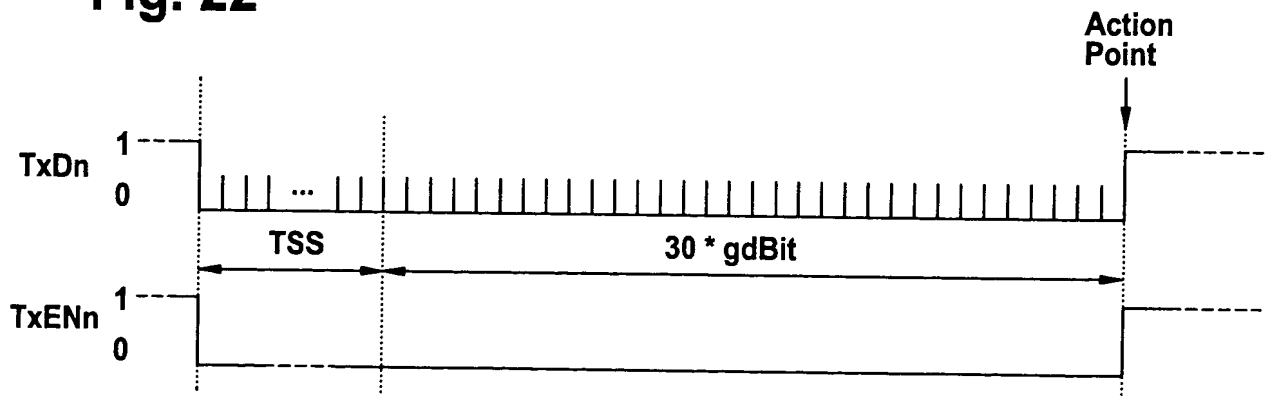
Fig. 20**Fig. 21****Fig. 22**

Fig. 23

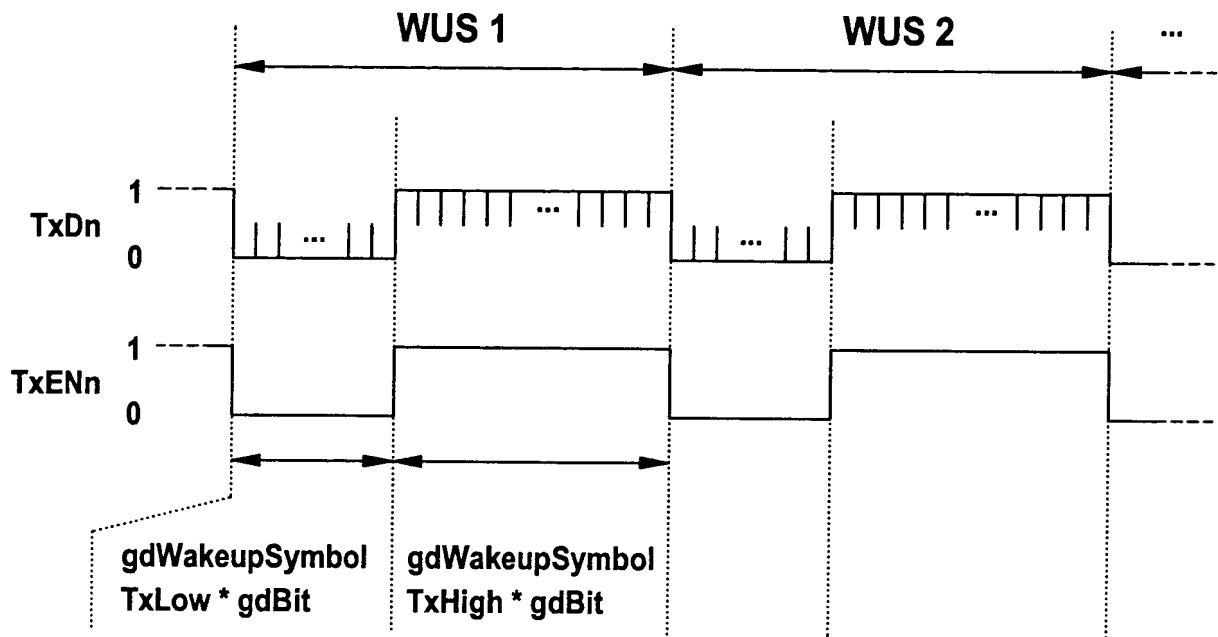


Fig. 24

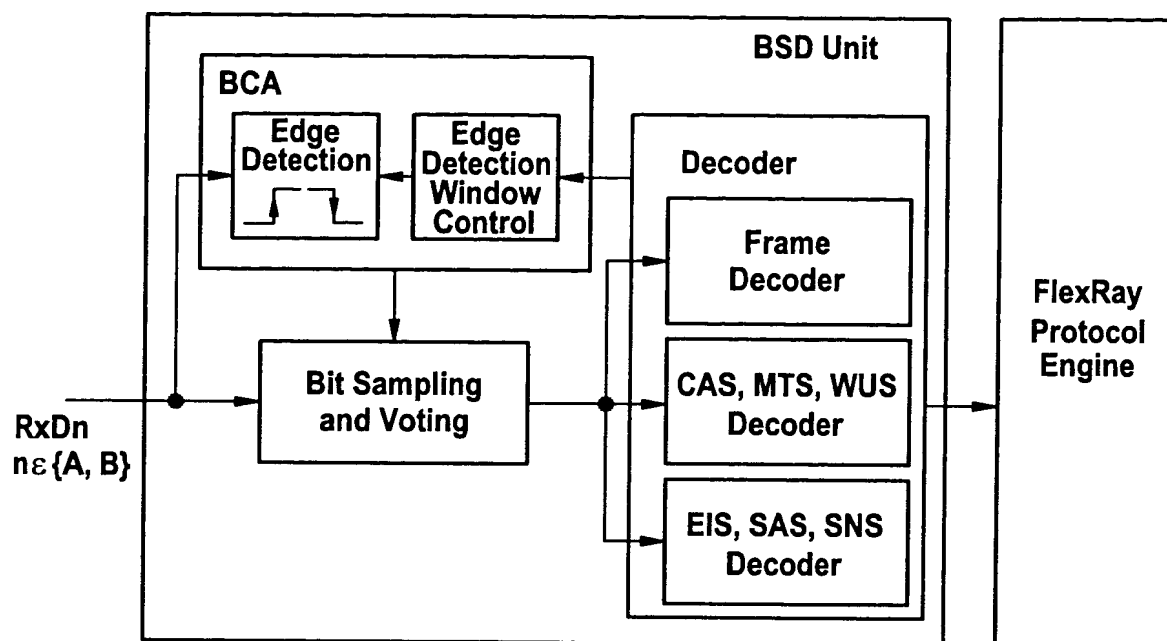


Fig. 25

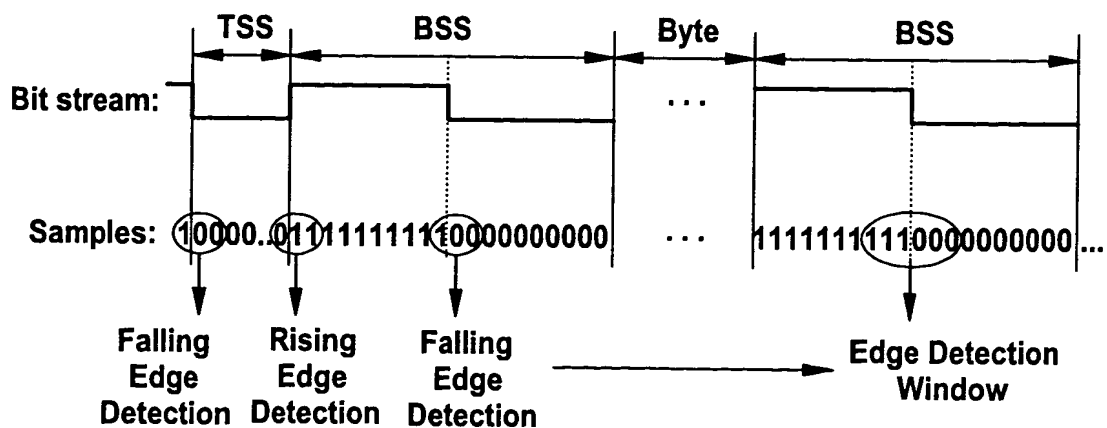


Fig. 26

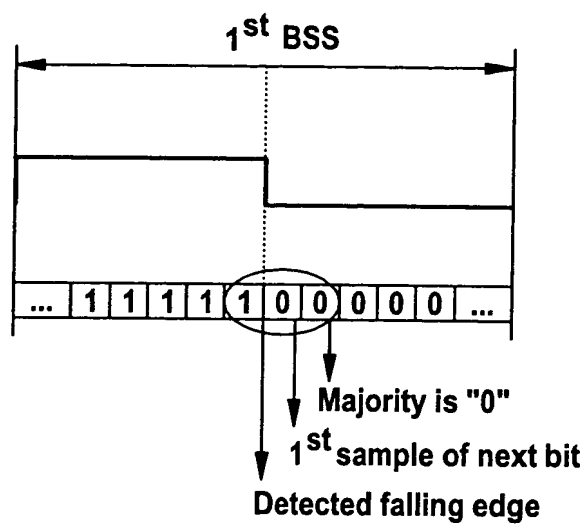


Fig. 27

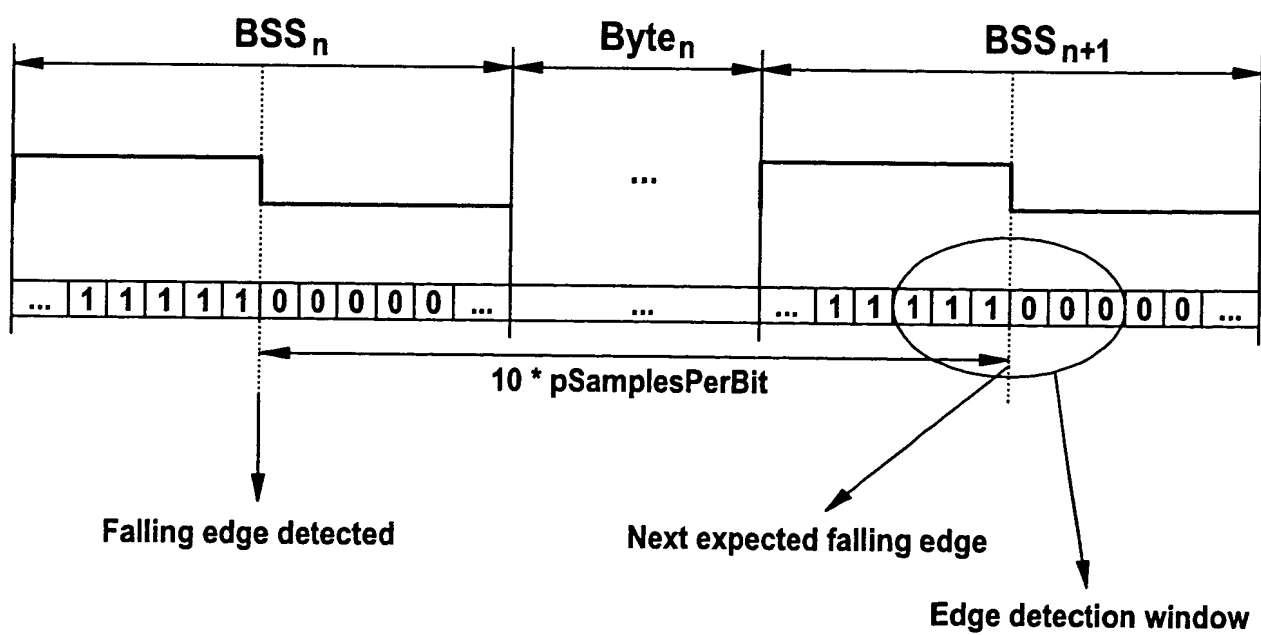


Fig. 28

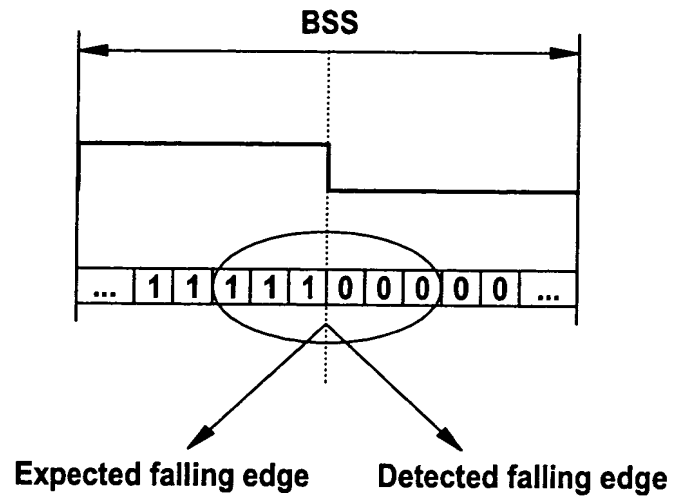


Fig. 29

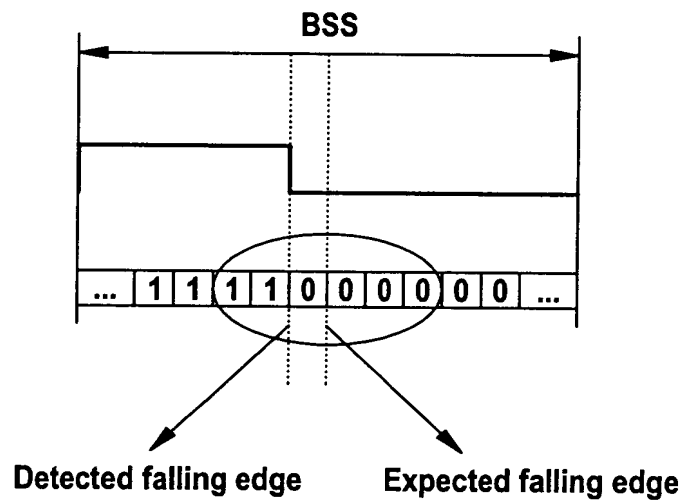


Fig. 30

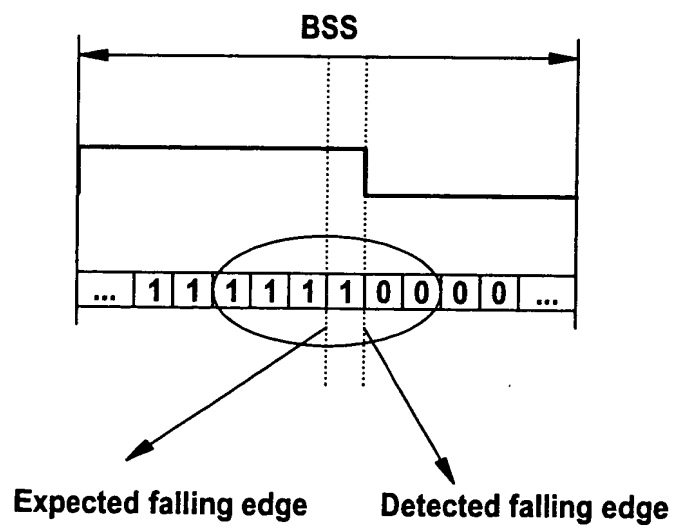


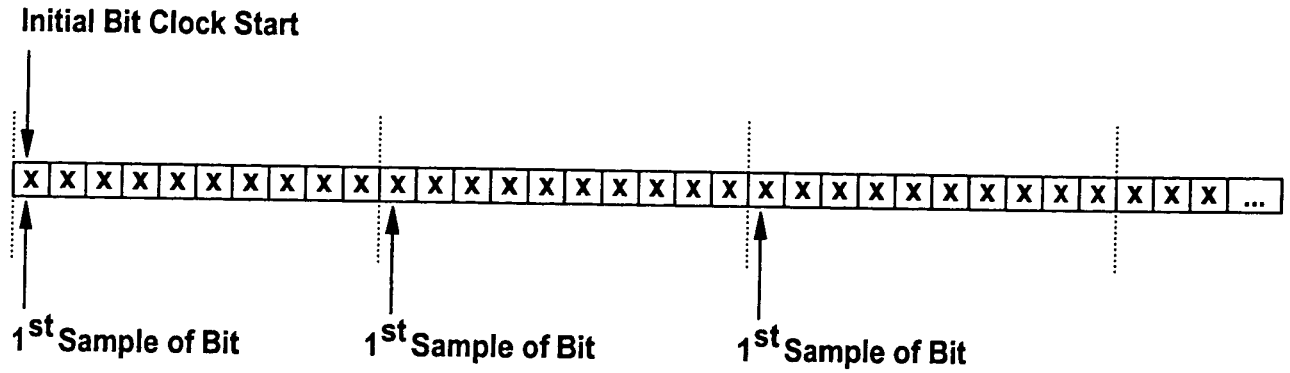
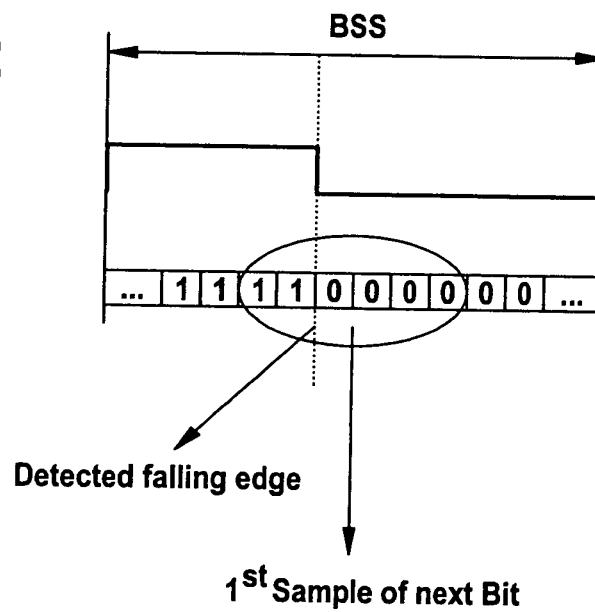
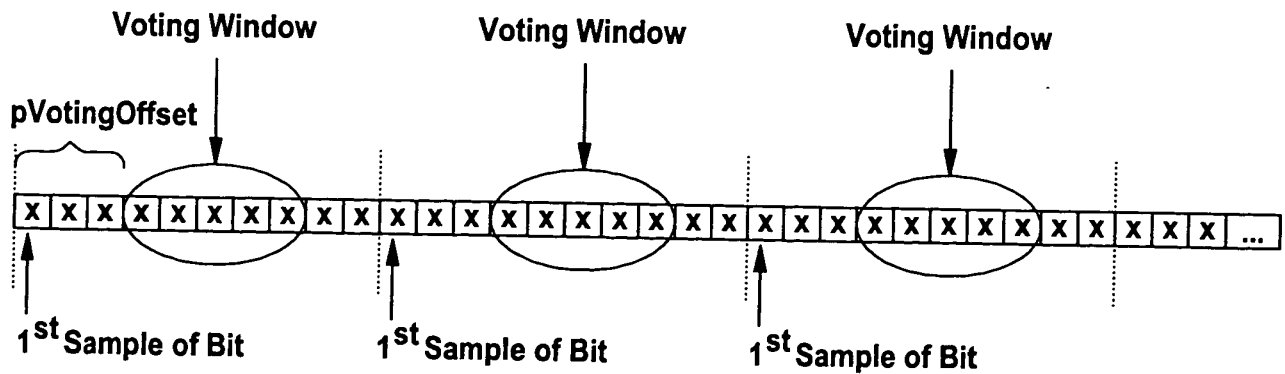
Fig. 31**Fig. 32****Fig. 33**

Fig. 34

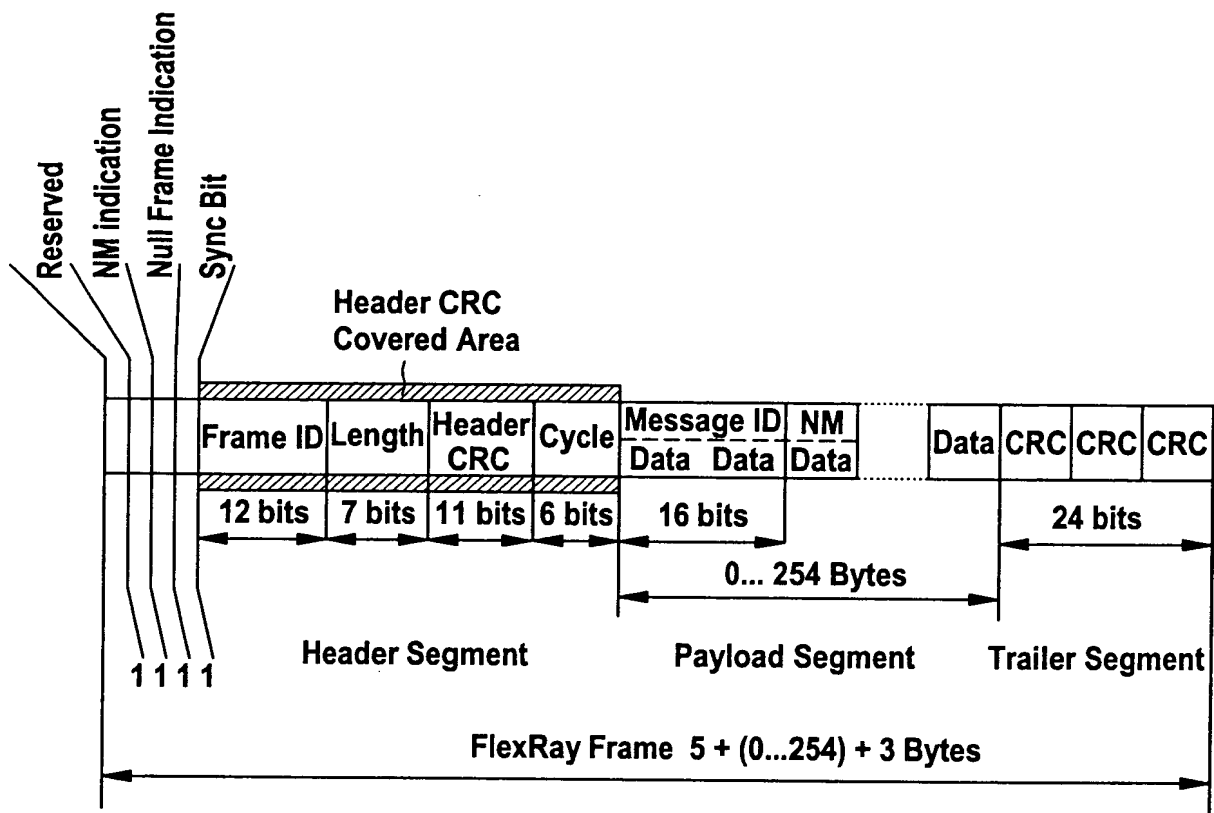


Fig. 35

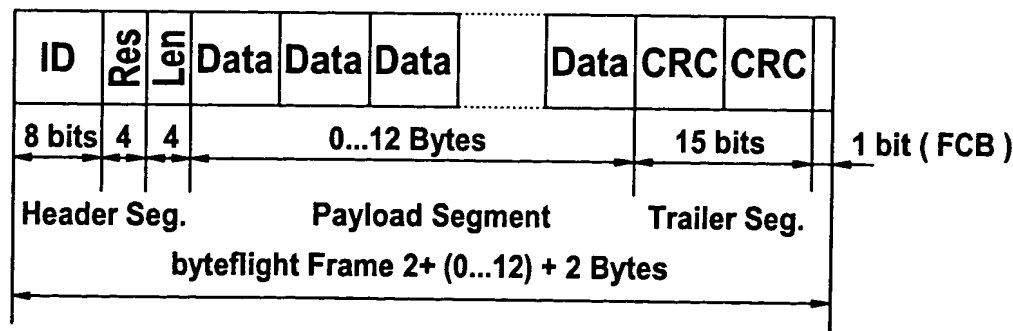


Fig. 36

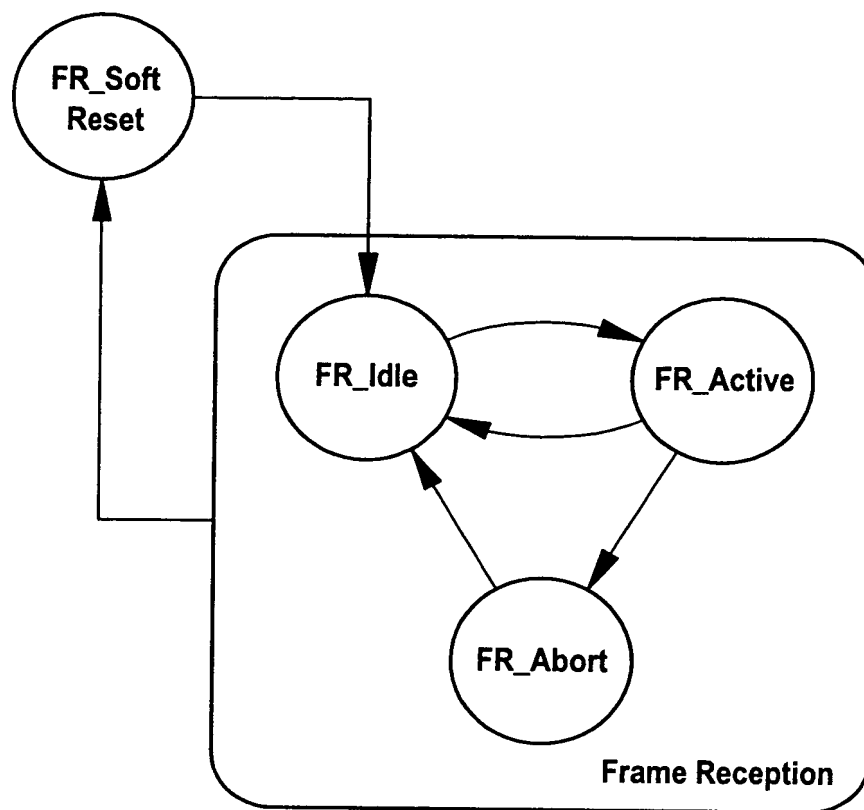


Fig. 37

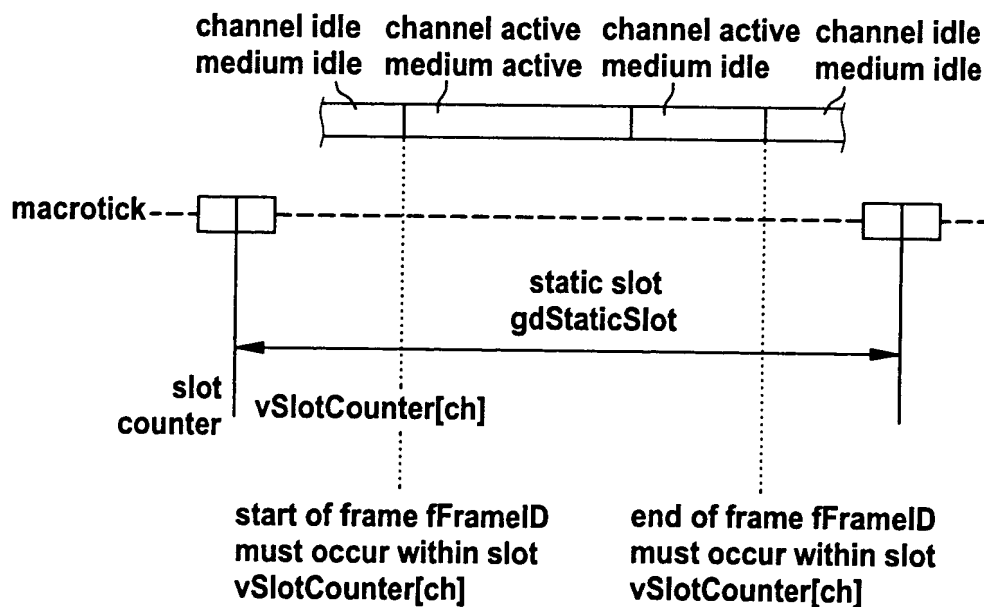


Fig. 38

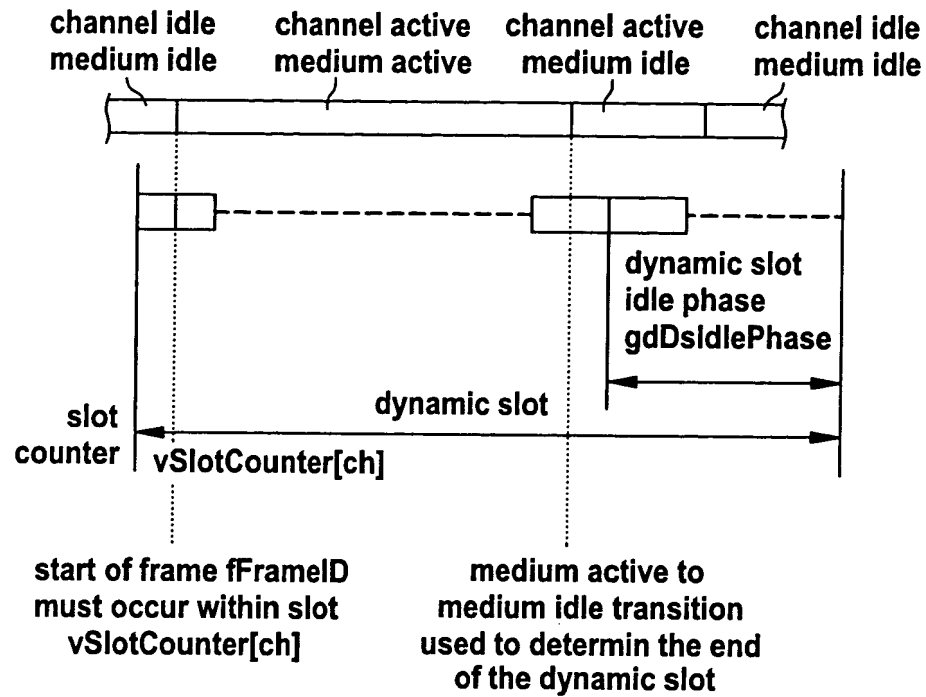


Fig. 39

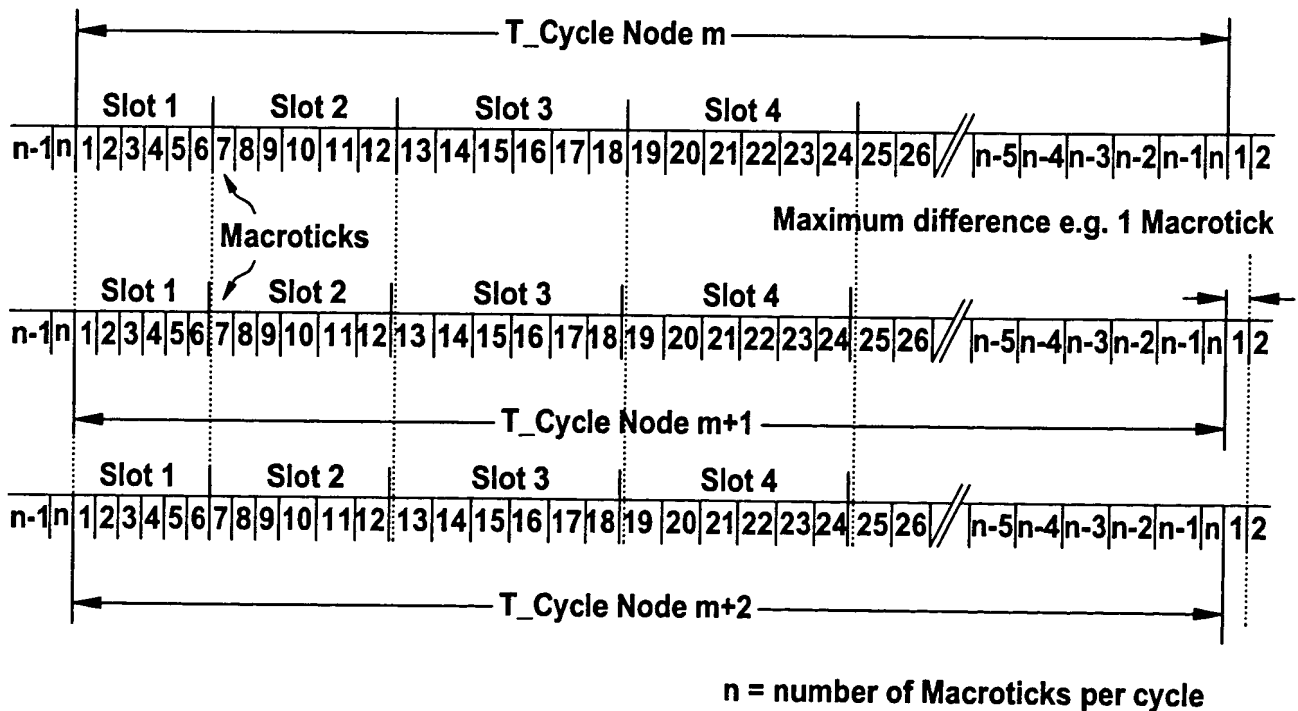


Fig. 40

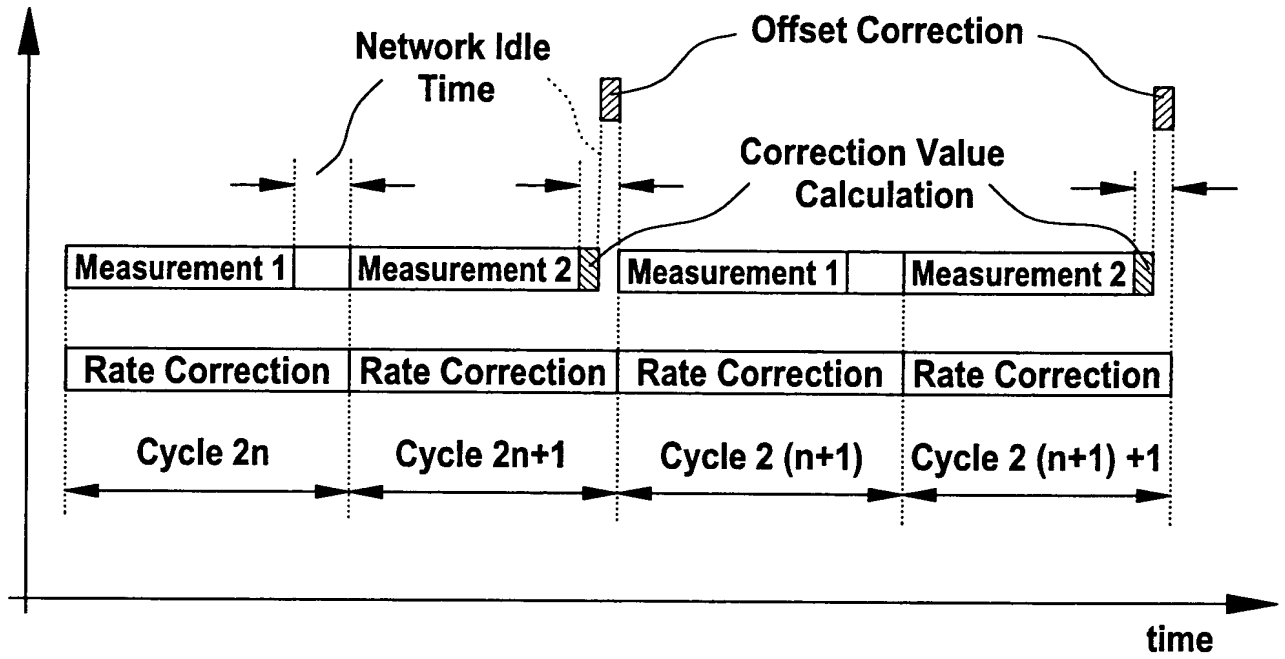


Fig. 41

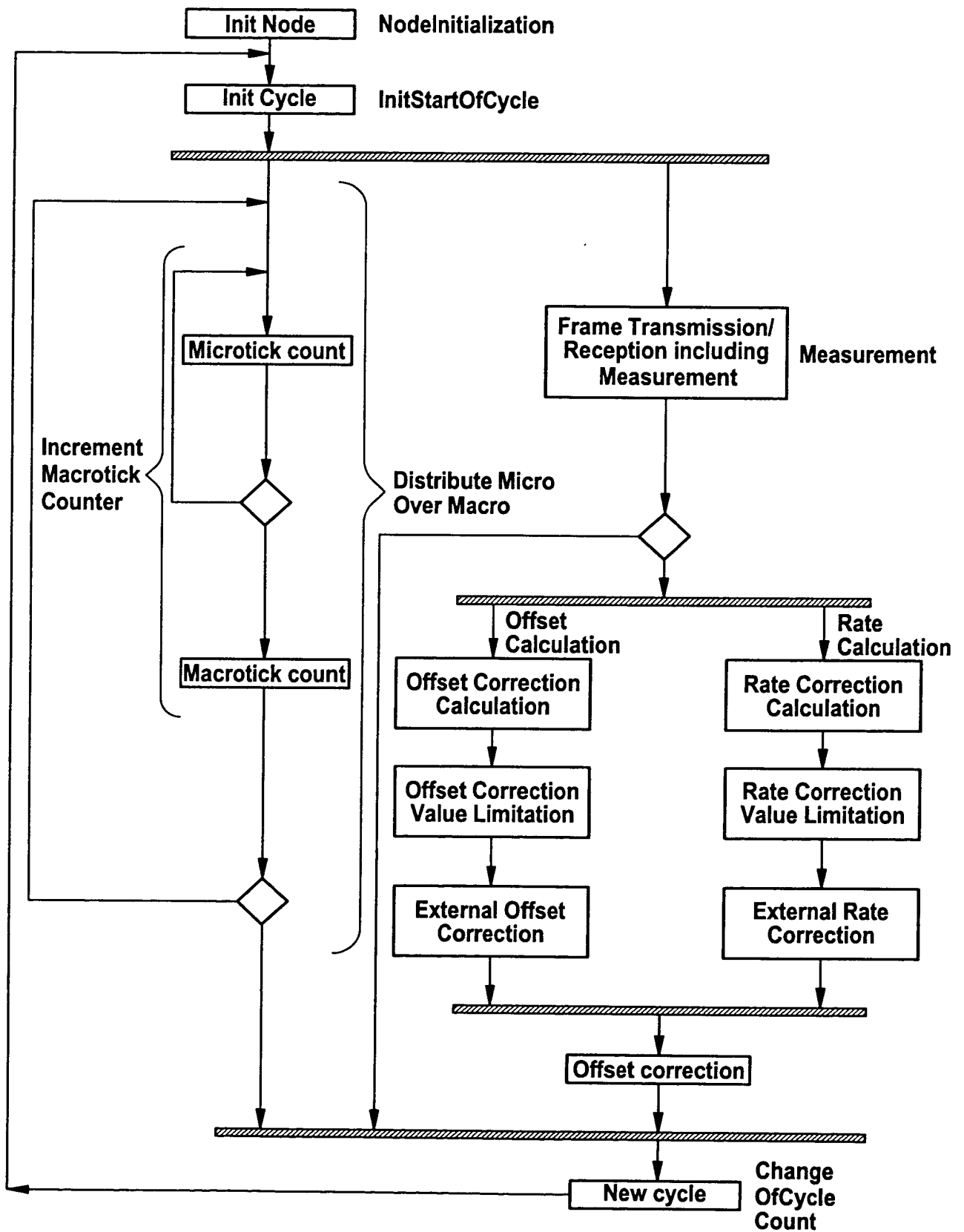


Fig. 42

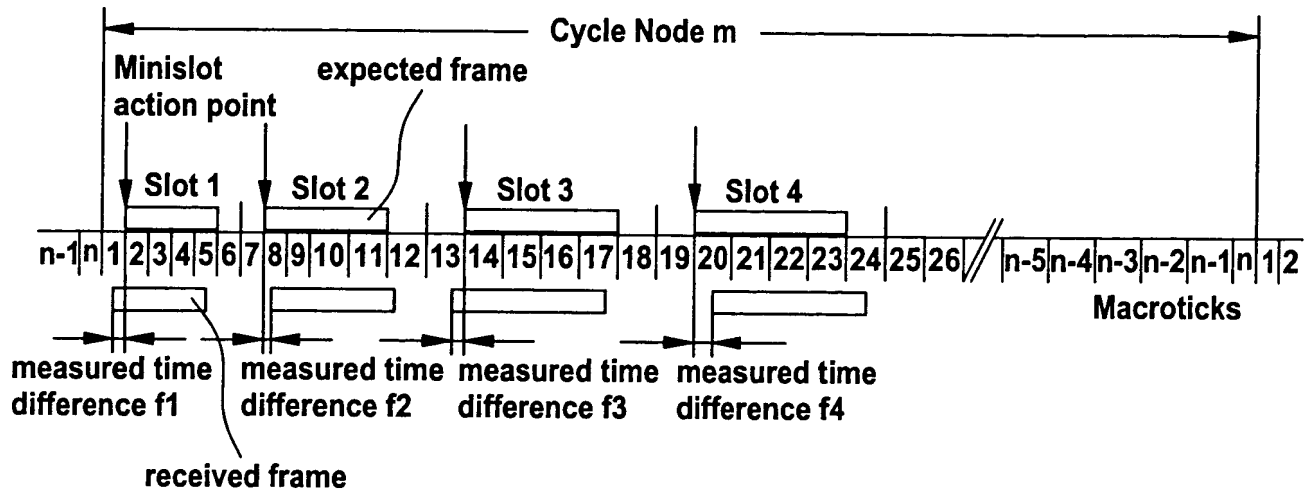


Fig. 43

$$\begin{array}{c}
 15 \\
 13 \\
 11 \\
 \dots \\
 6 \\
 3 \\
 5
 \end{array}
 \rightarrow + \rightarrow 17 / 2 = 8$$

Fig. 44

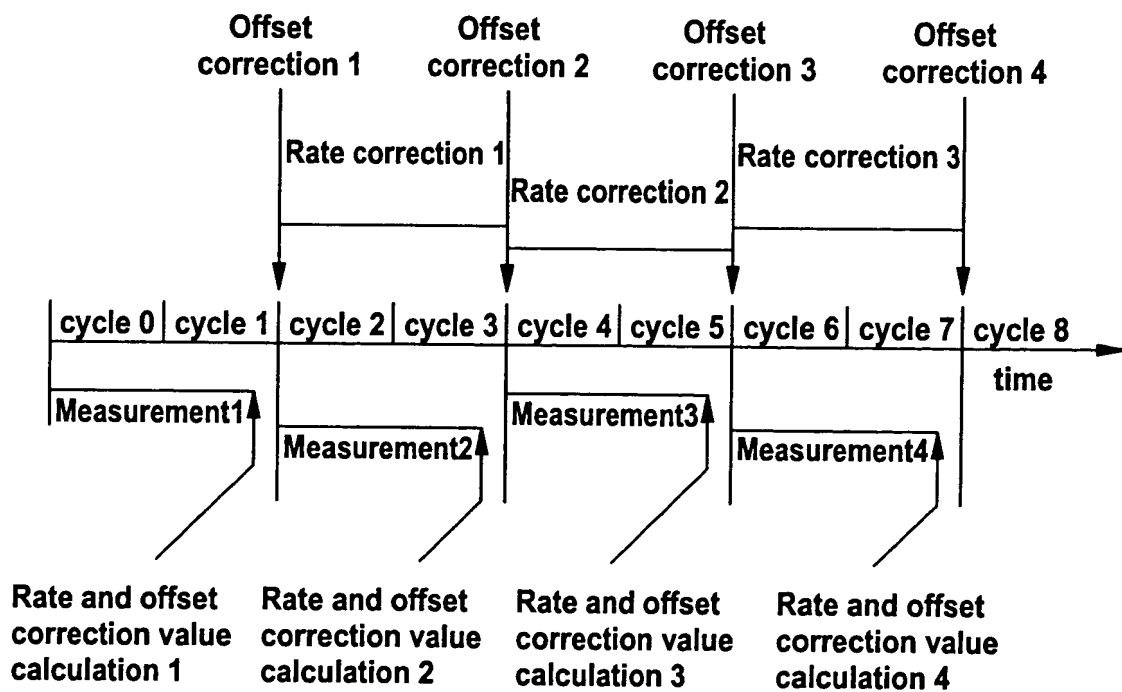


Fig. 45

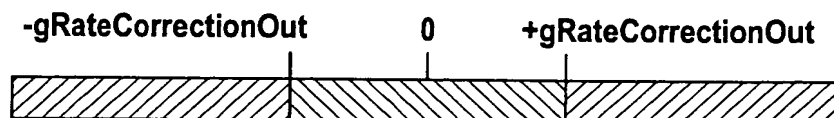


Fig. 46

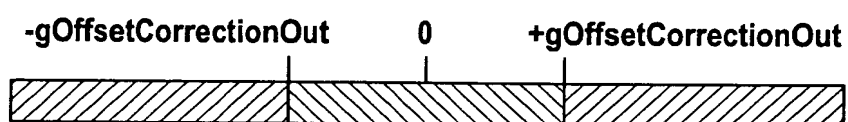


Fig. 47

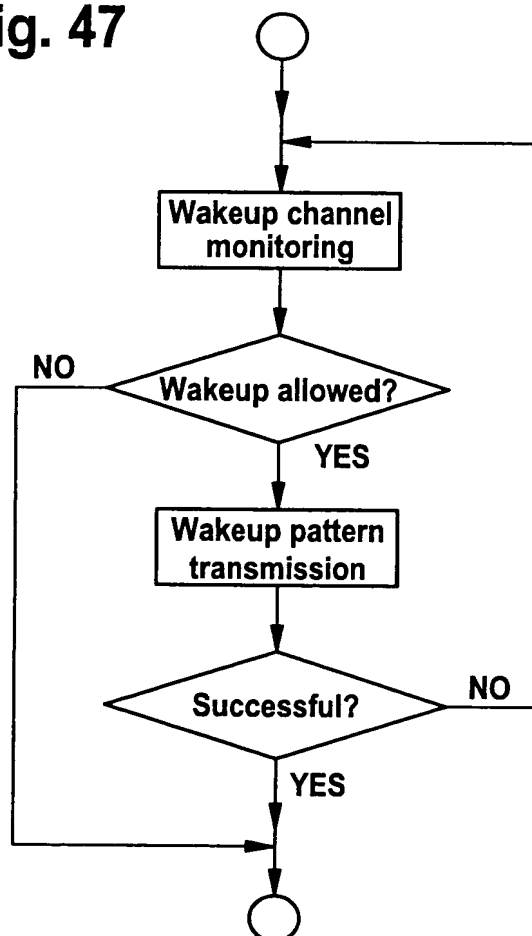


Fig. 48

Wakeup channel monitoring

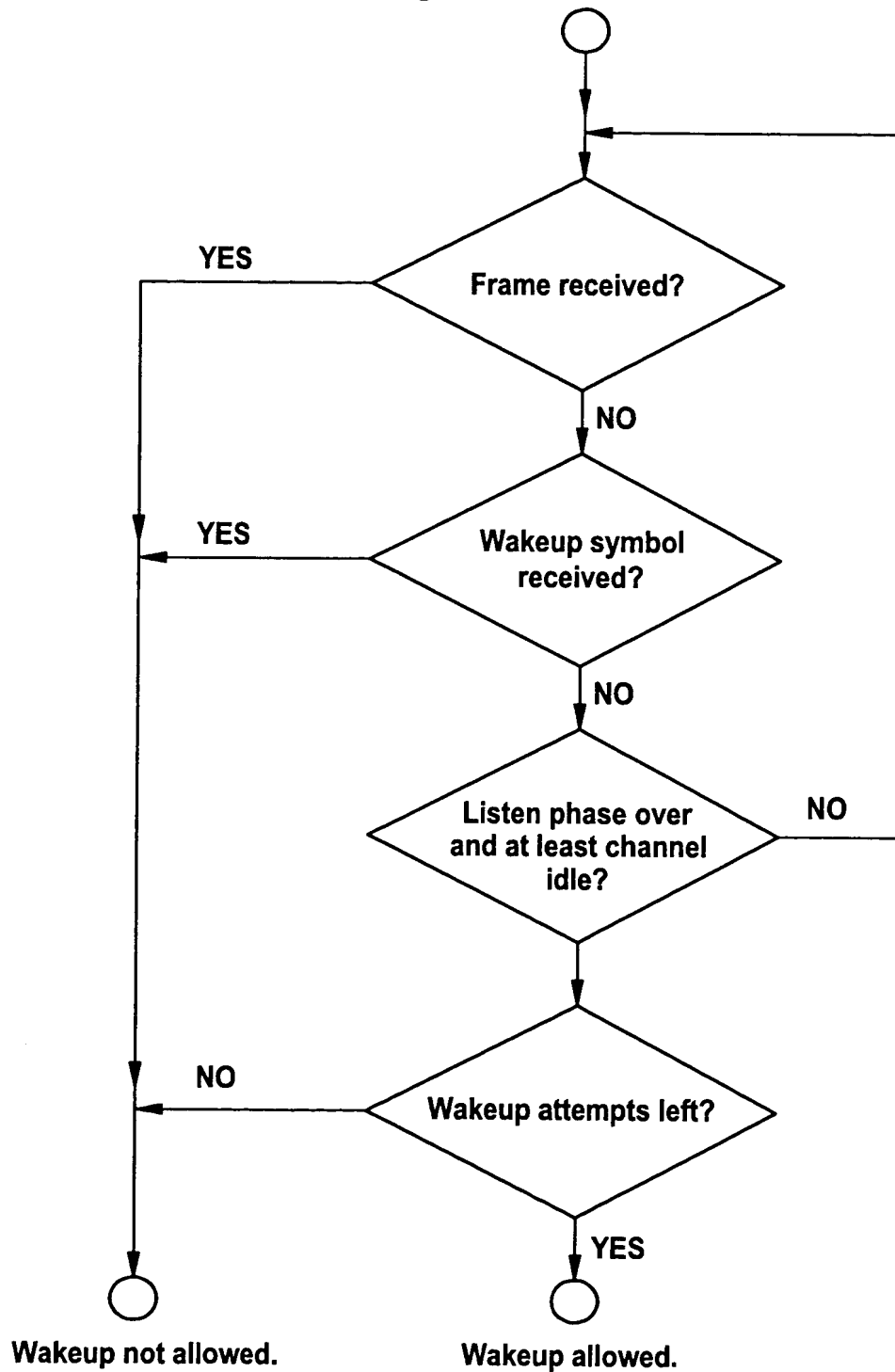


Fig. 49

Wakeup pattern transmission

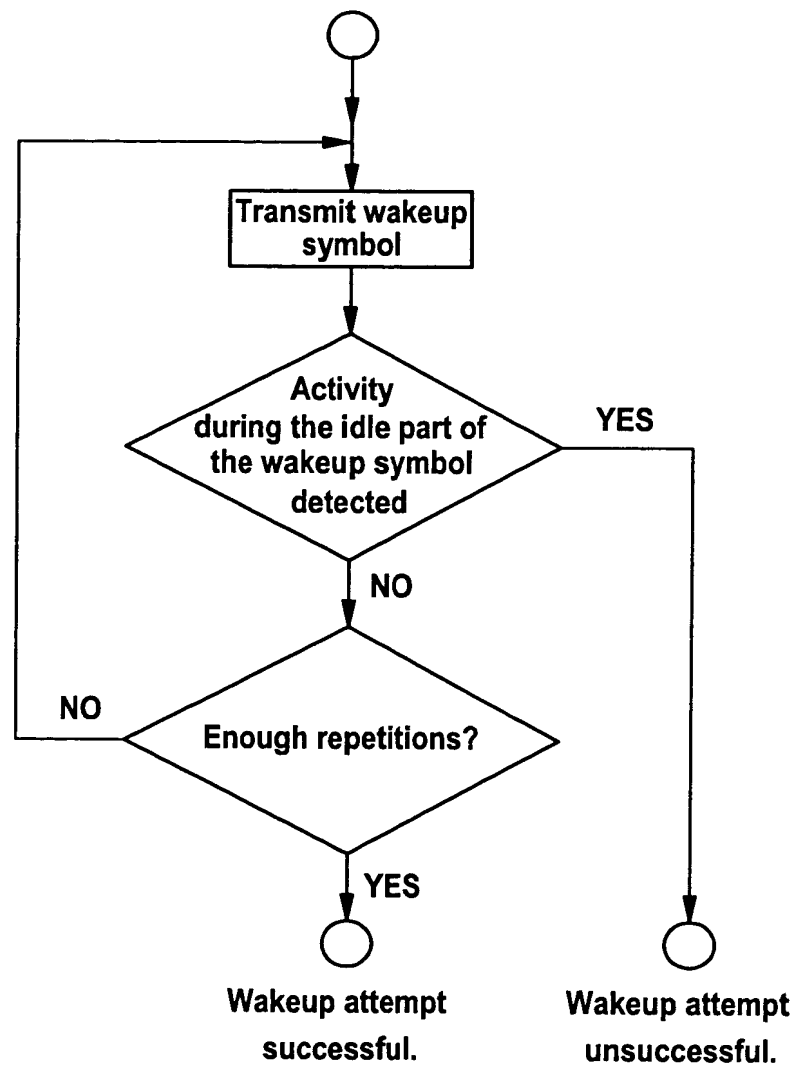


Fig. 50

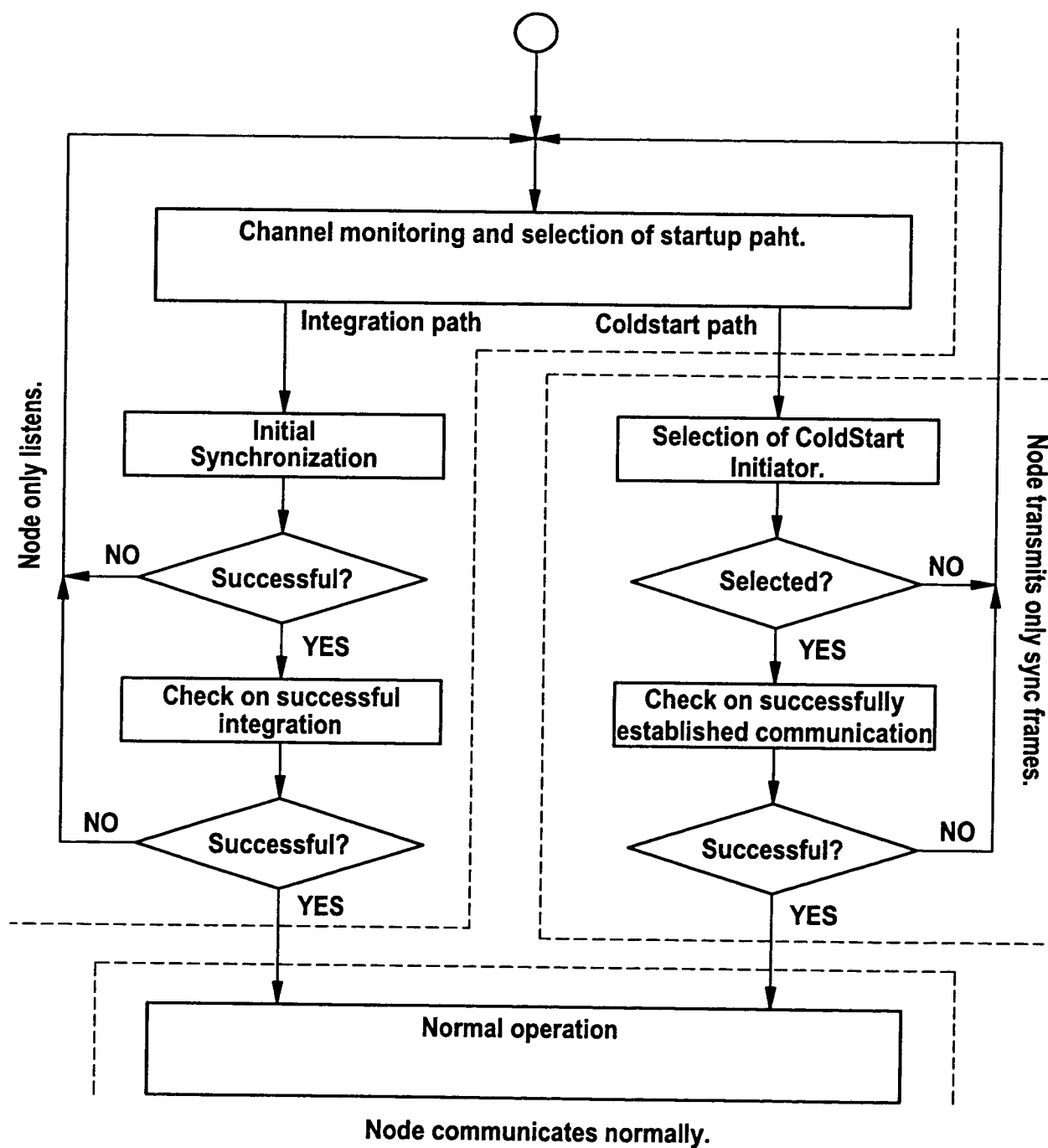


Fig. 51

Channel monitoring and selection of startup path.

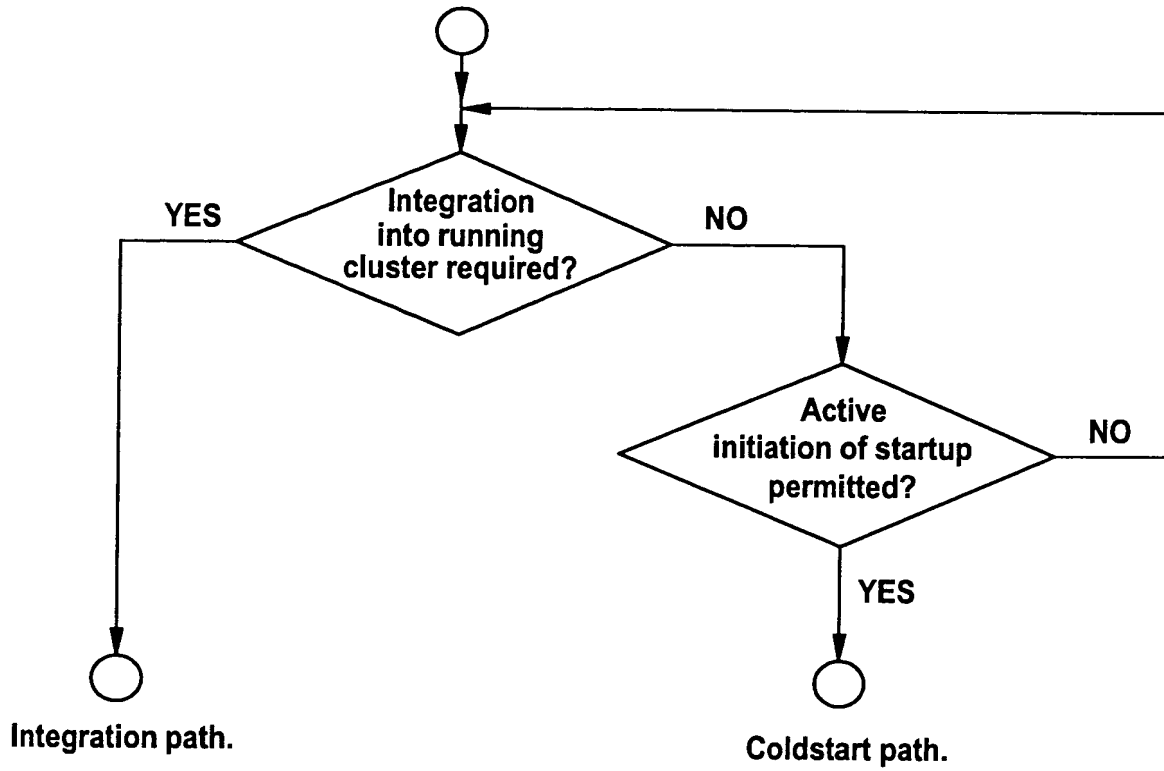


Fig. 52

Selection of ColdStart Initiator

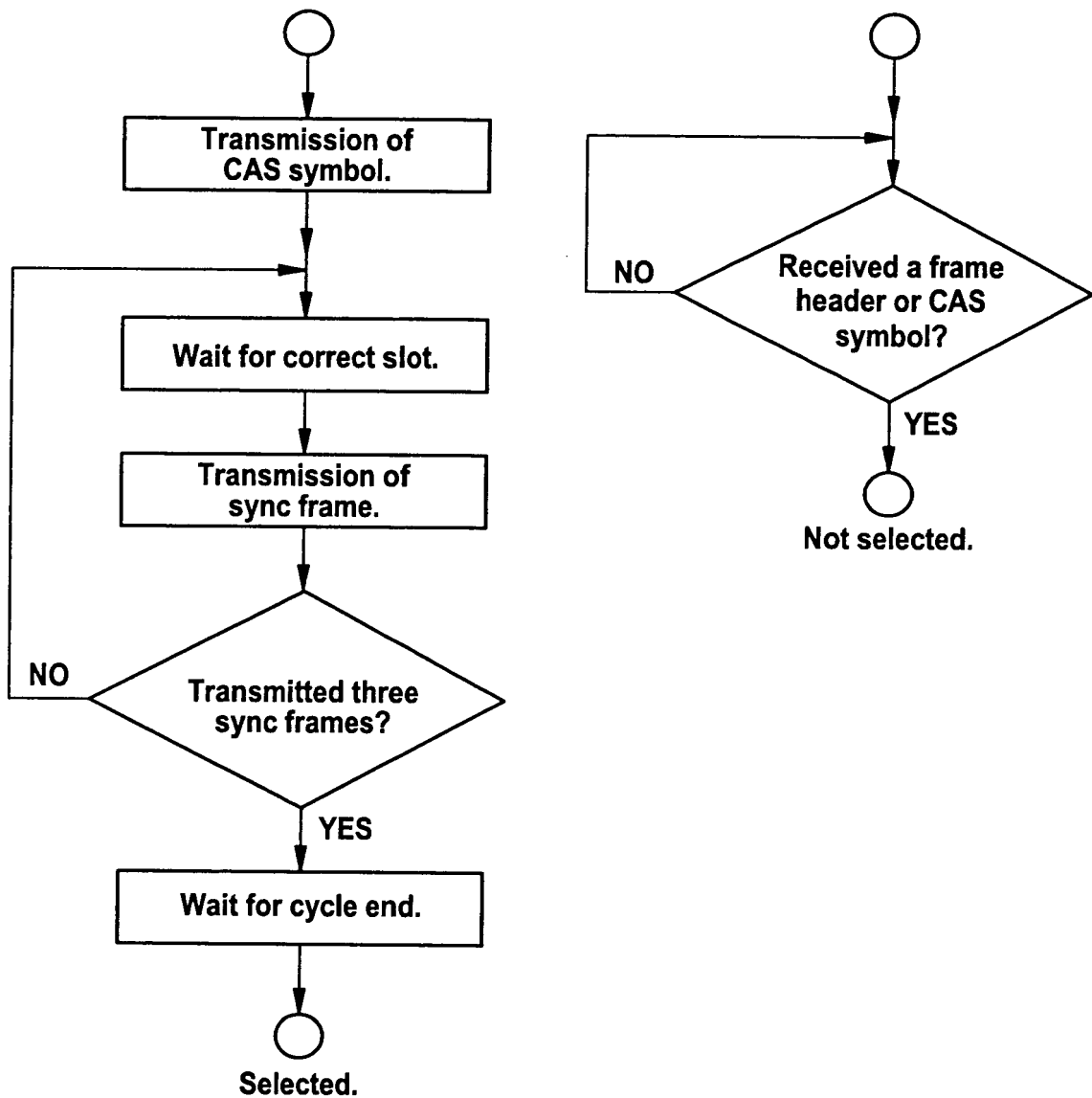


Fig. 53

Check on successfully established communication

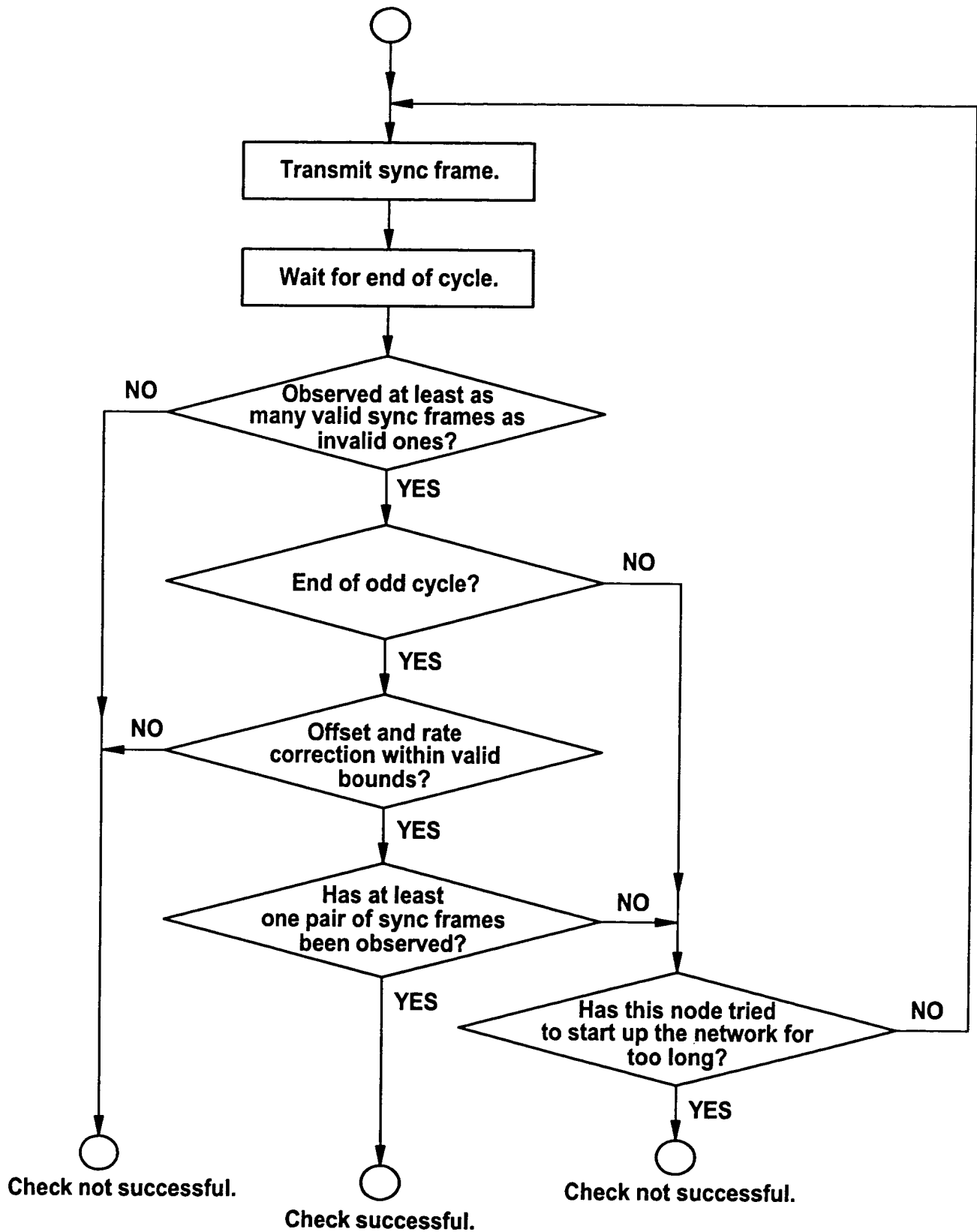


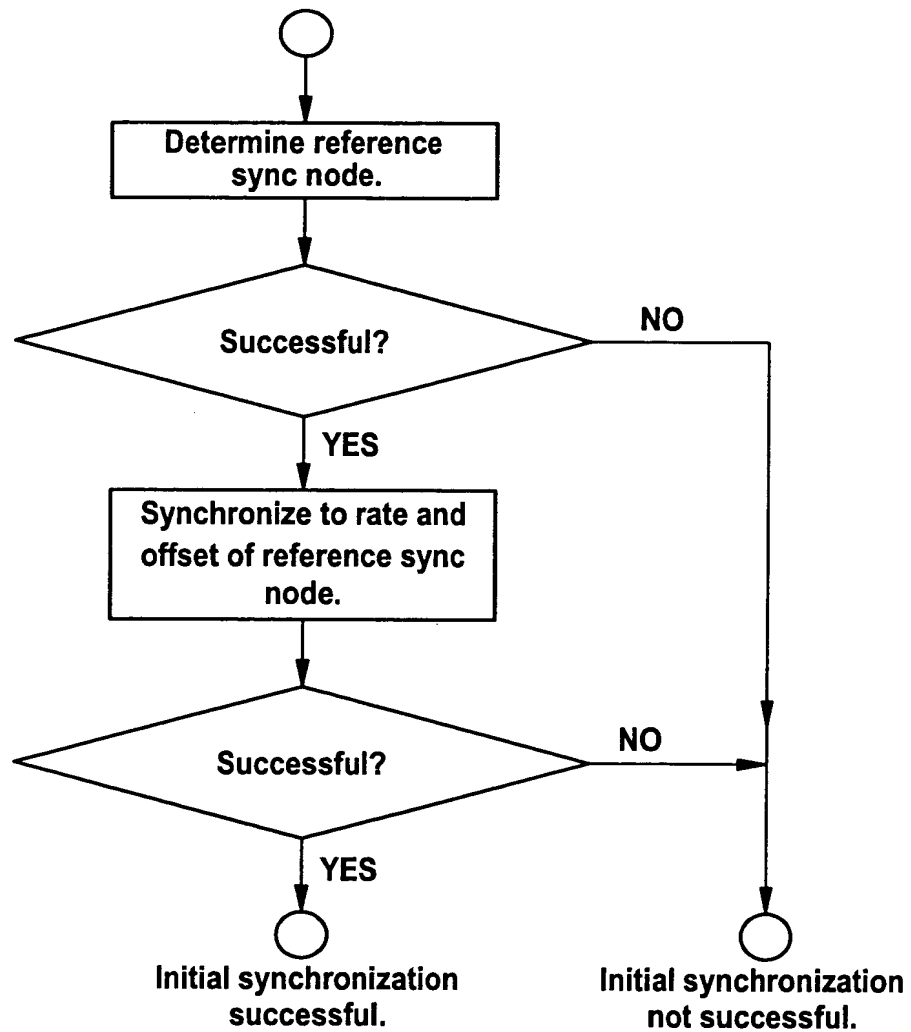
Fig. 54**Initial Synchronization**

Fig. 55

Check on successful integration

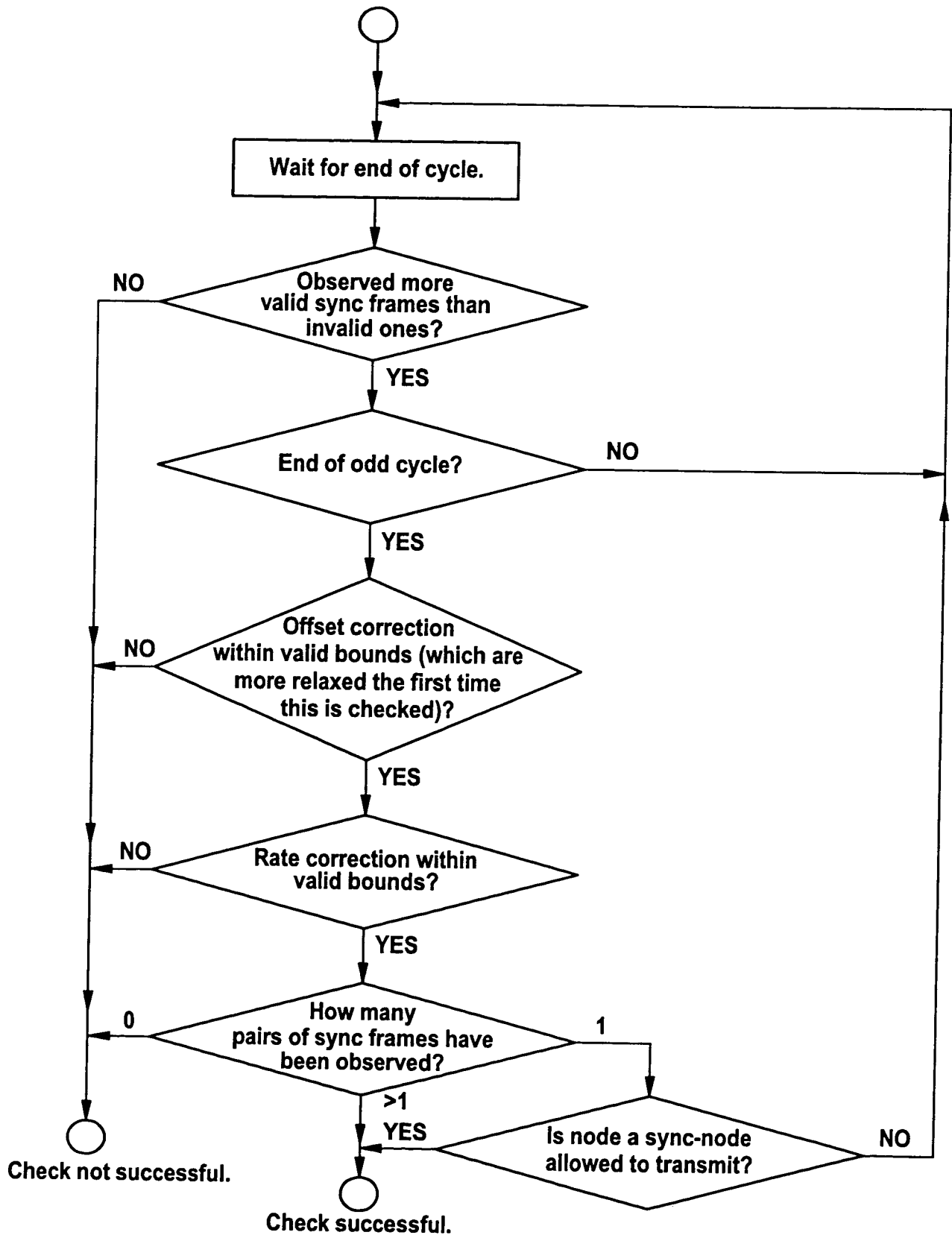


Fig. 56

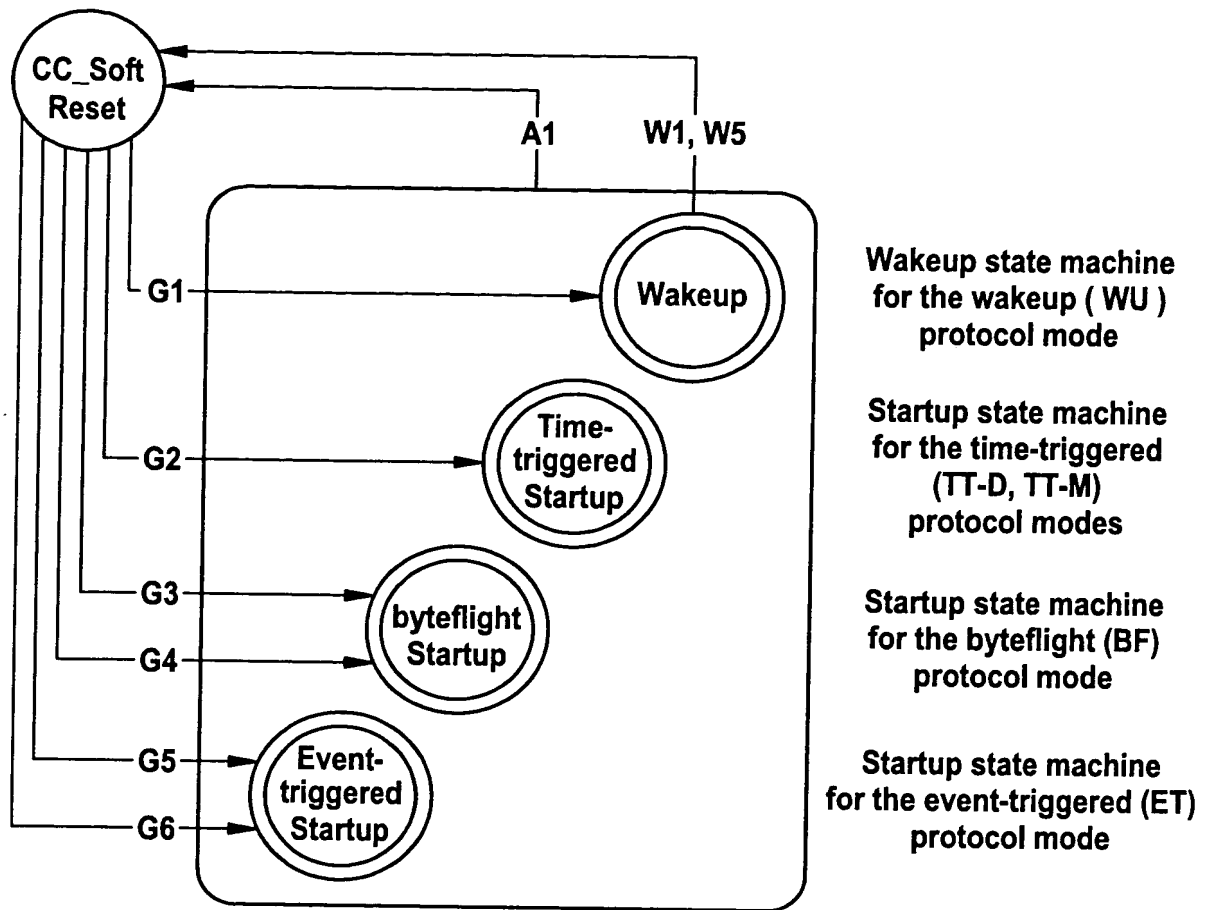


Fig. 57

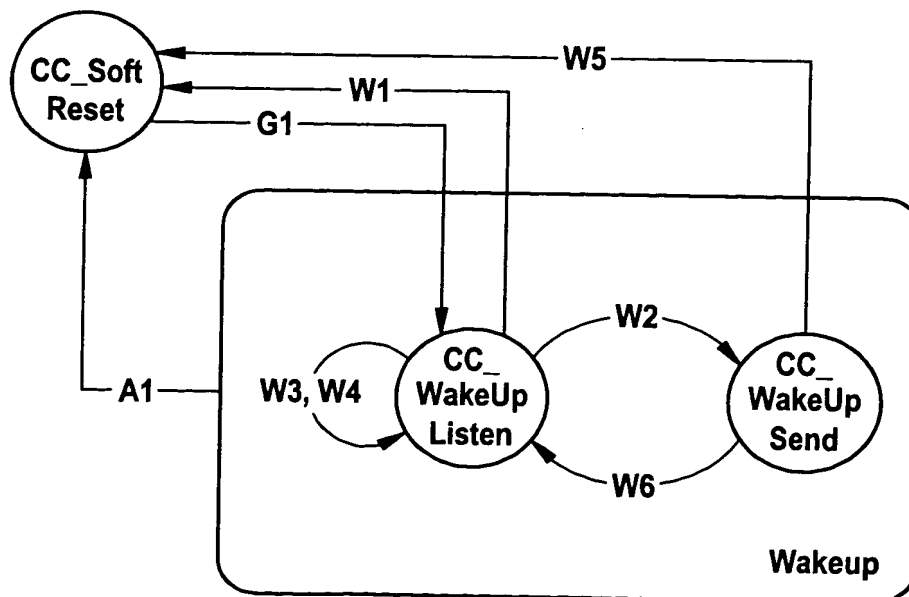


Fig. 58

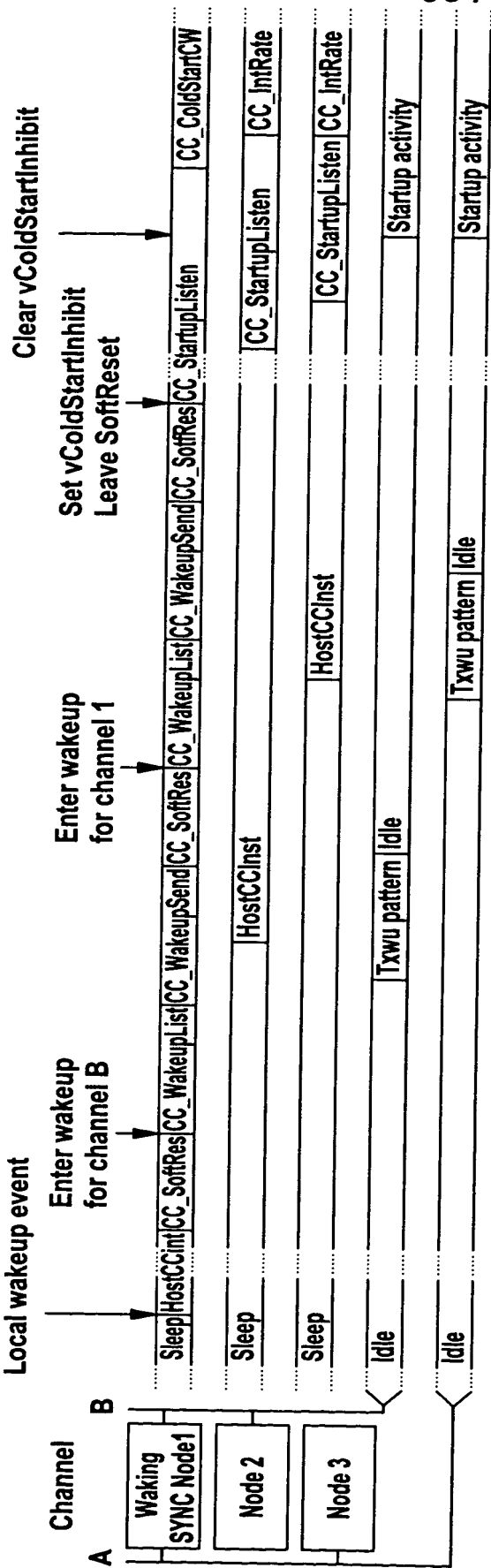


Fig. 59

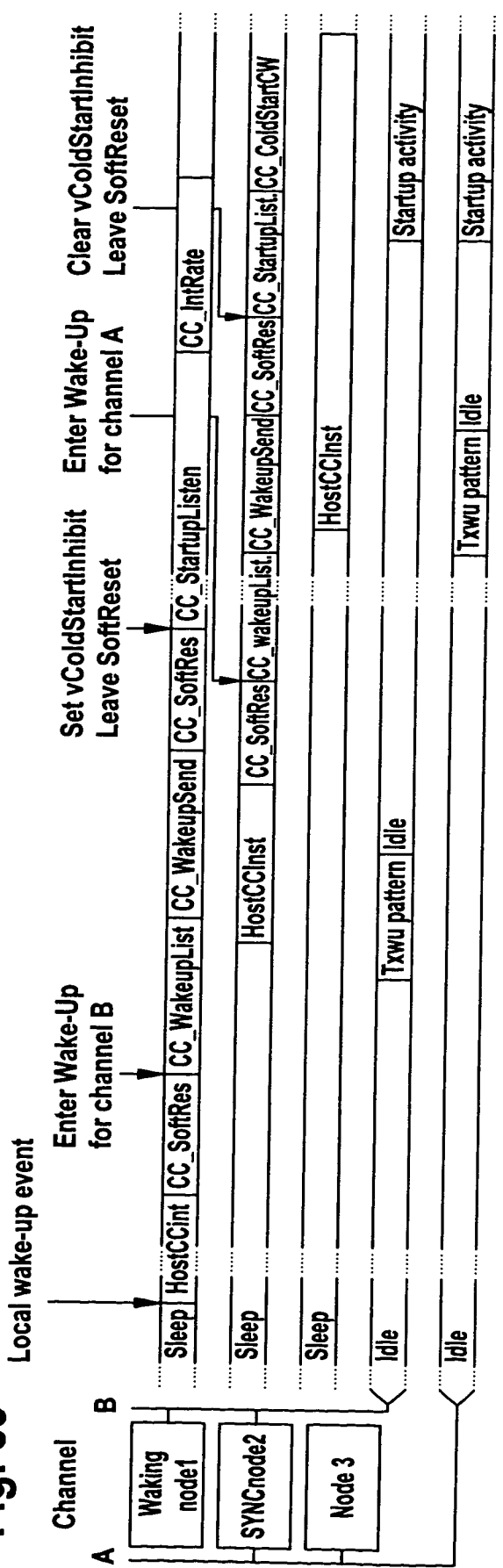


Fig. 60

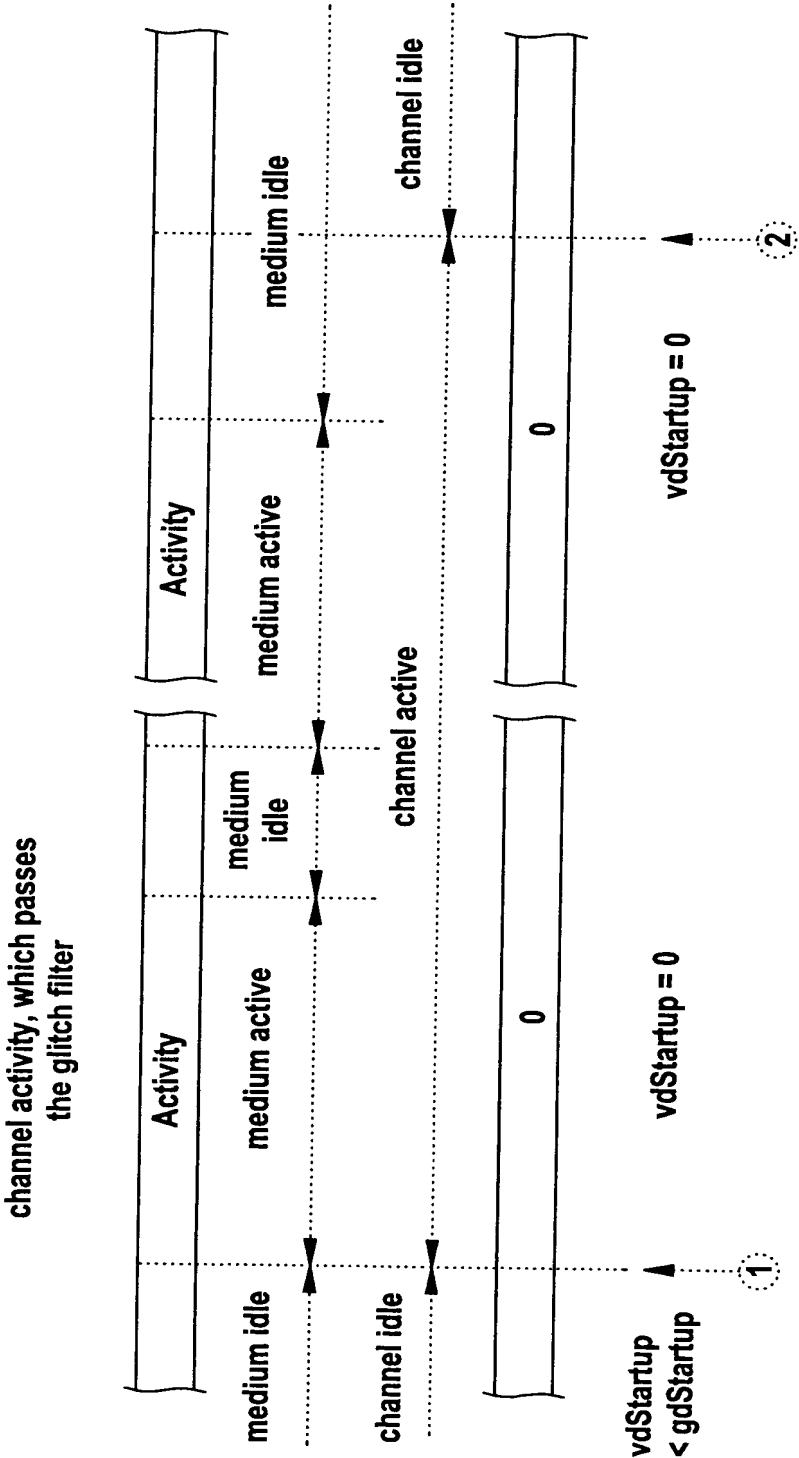


Fig. 61

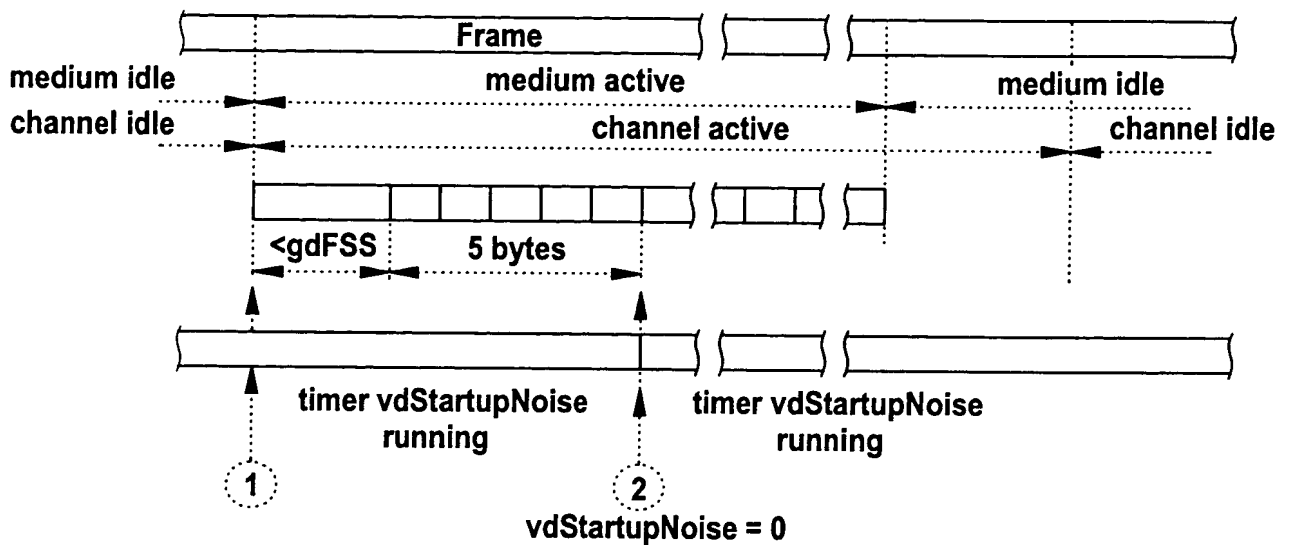


Fig. 62

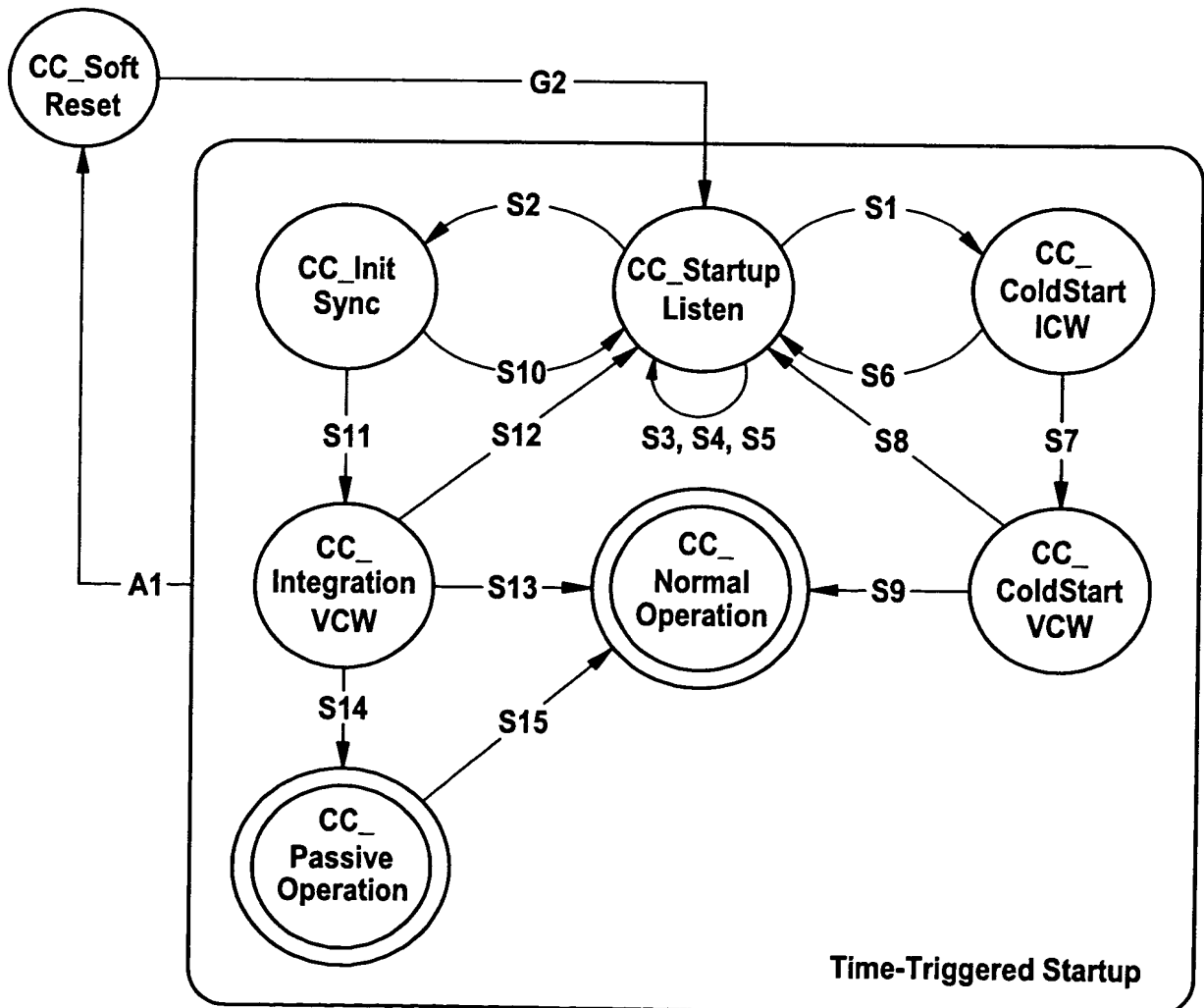


Fig. 63

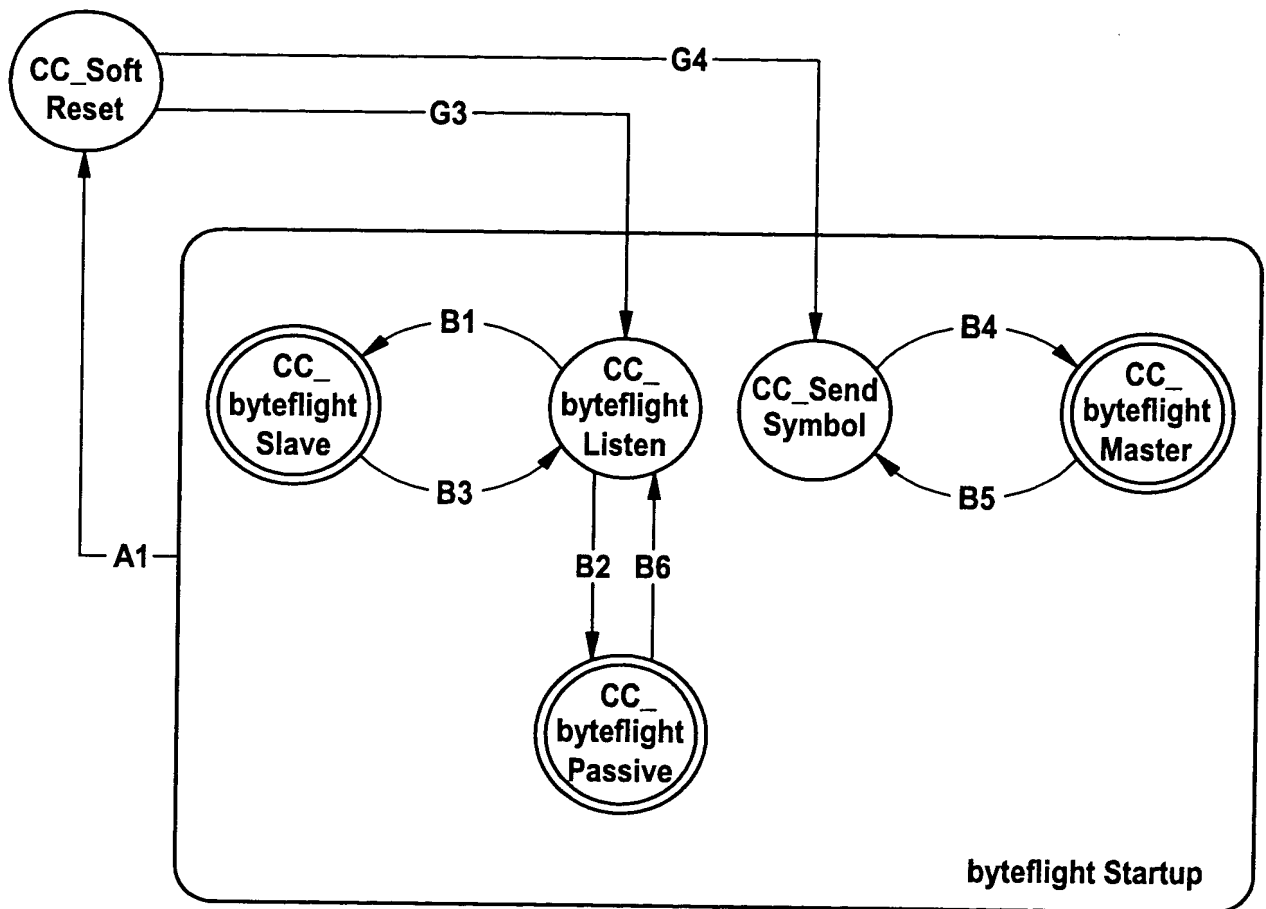


Fig. 64

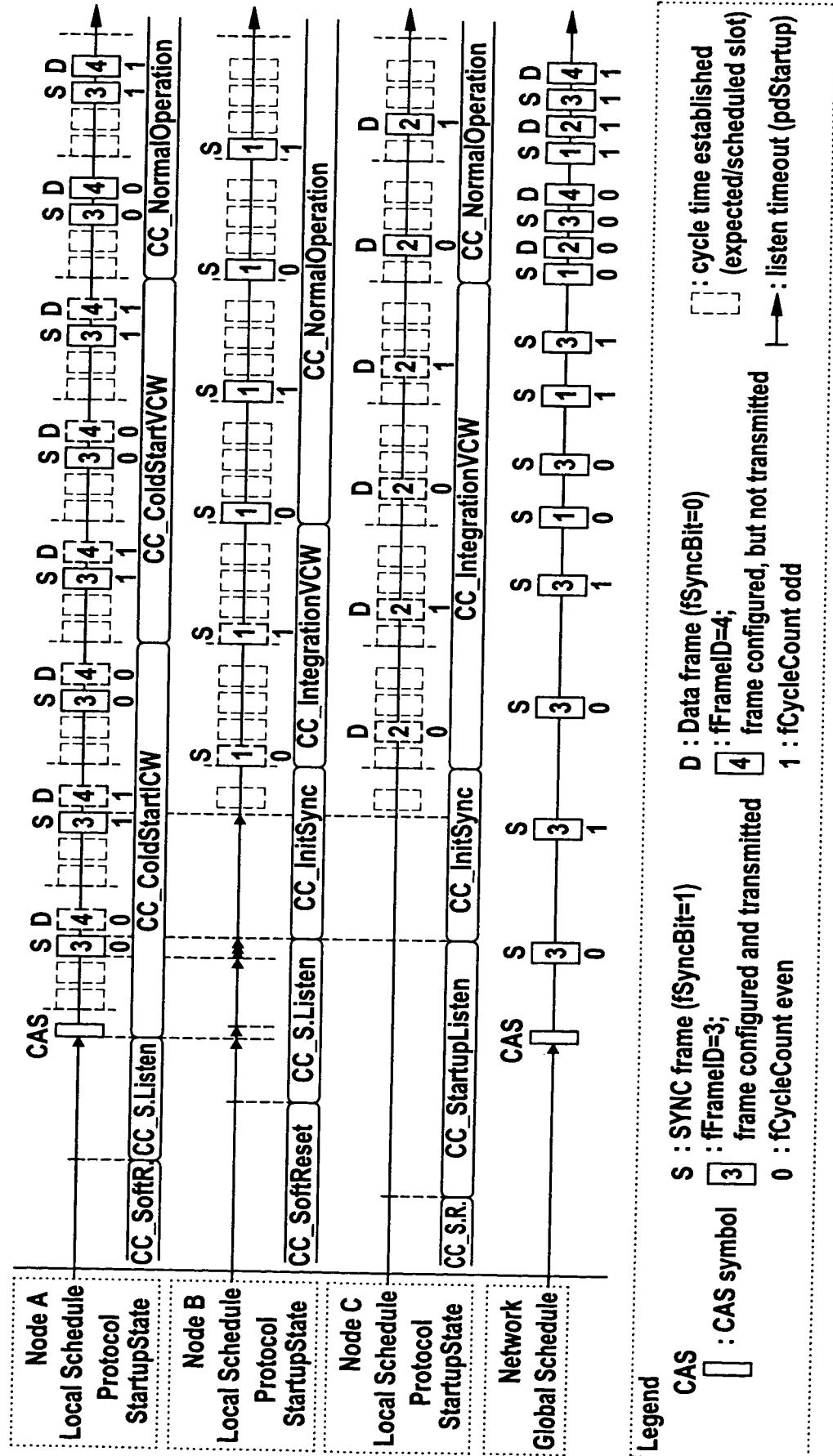


Fig. 65

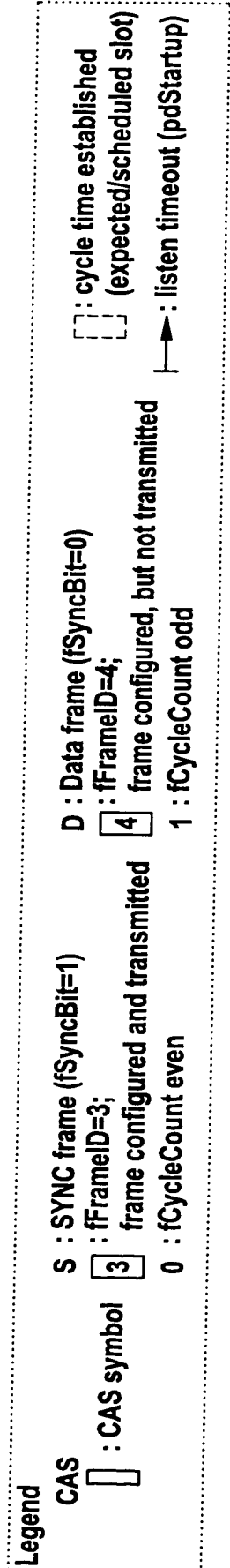
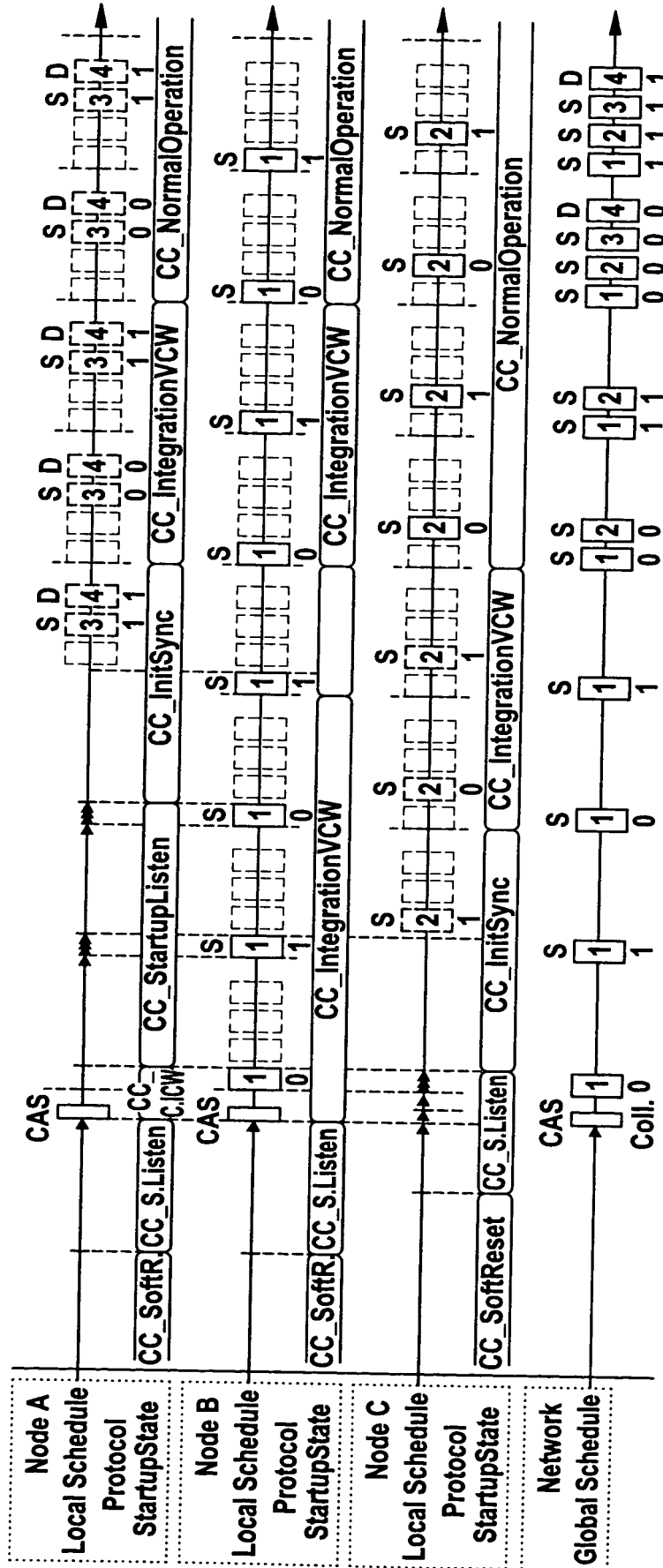


Fig. 66

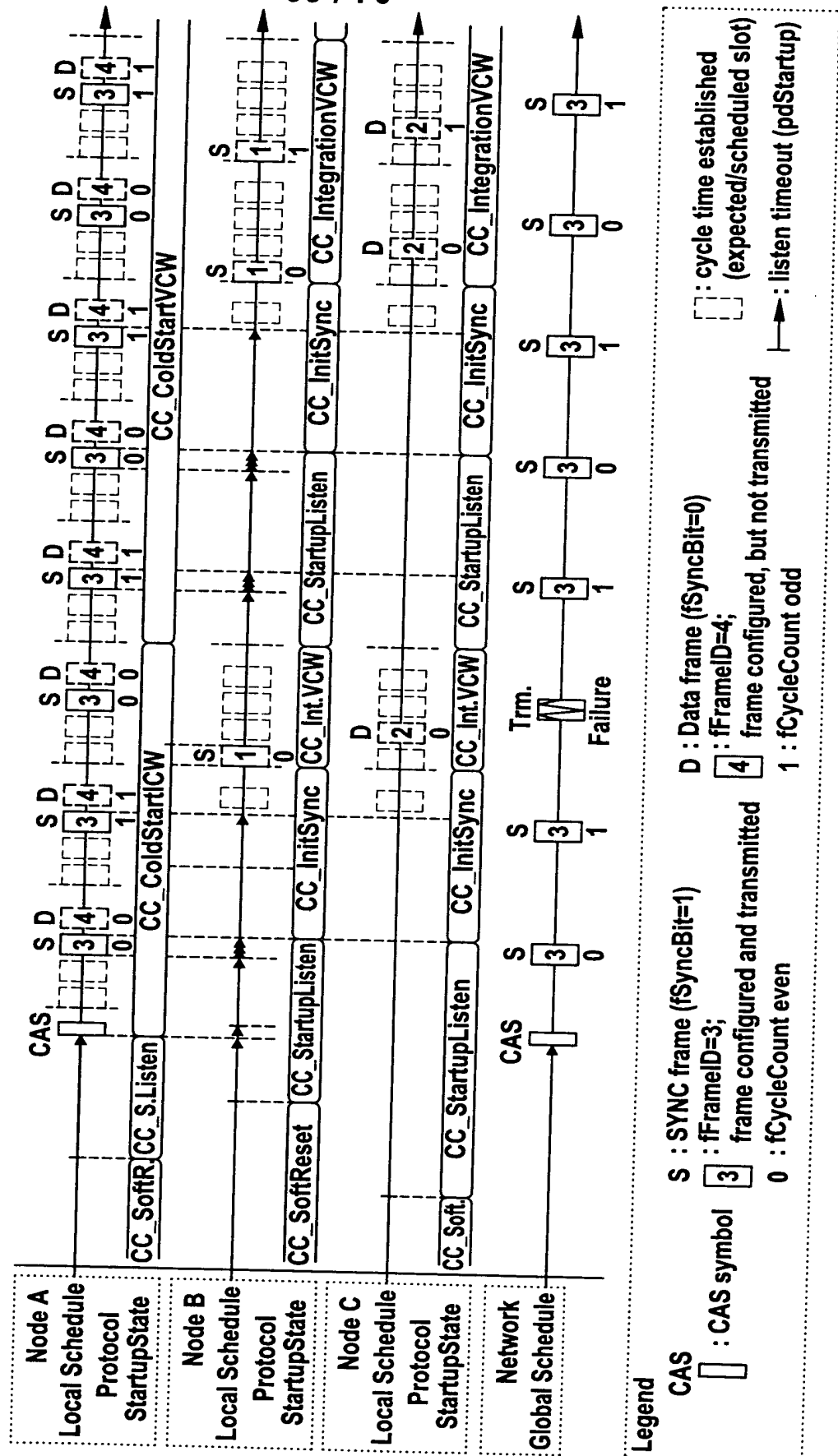


Fig. 67

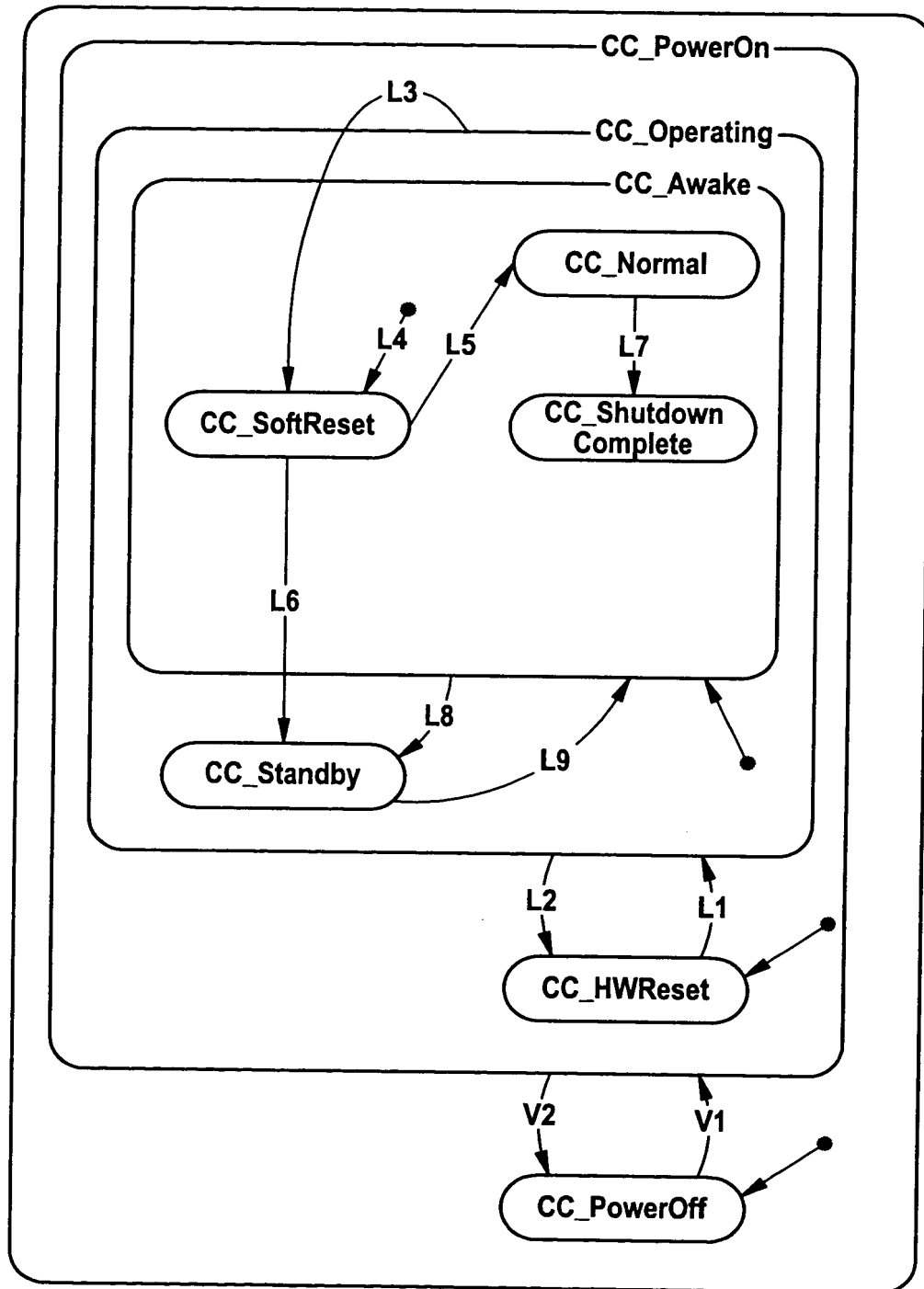


Fig. 68

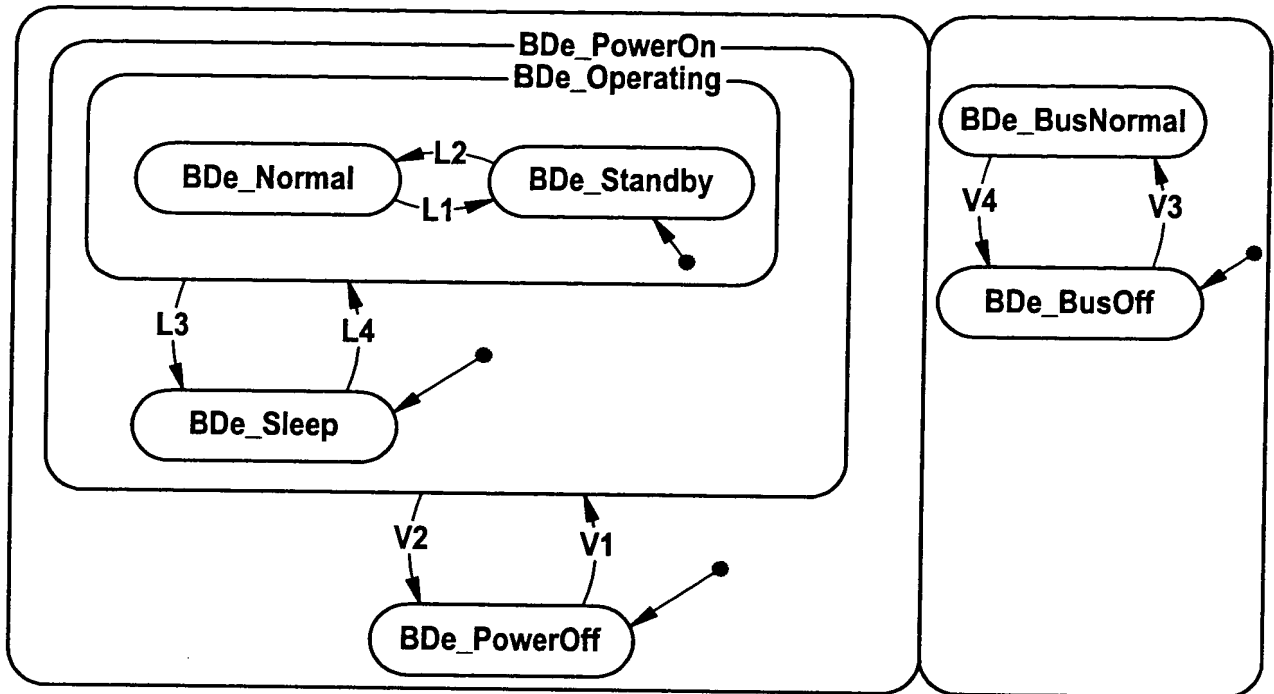


Fig. 69

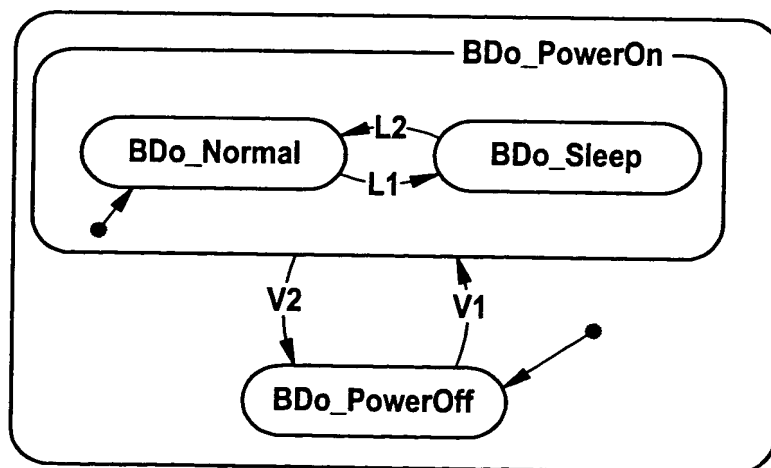


Fig. 70

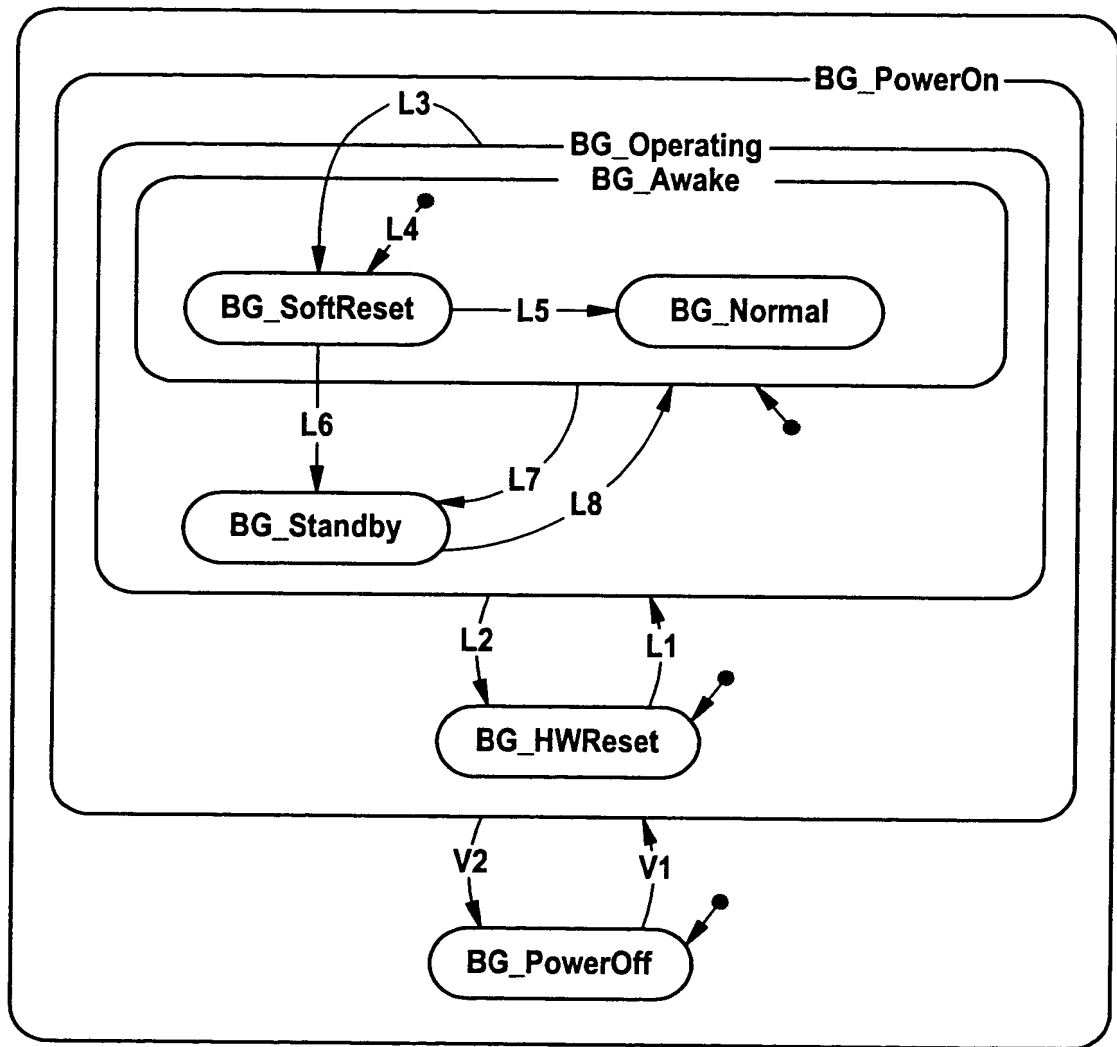


Fig. 71

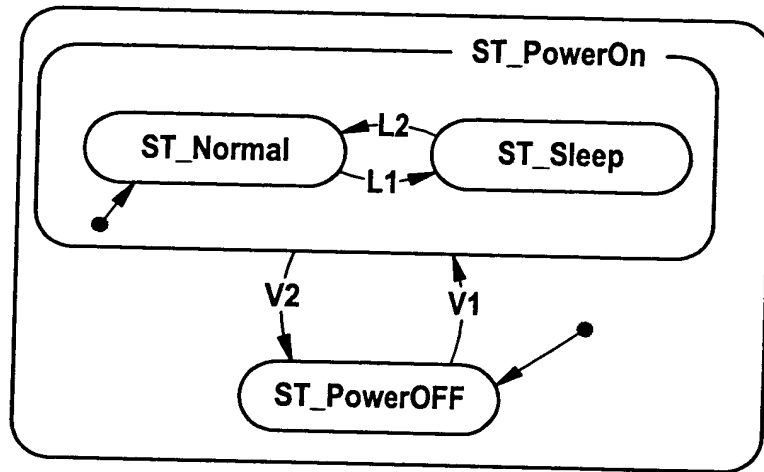


Fig. 72

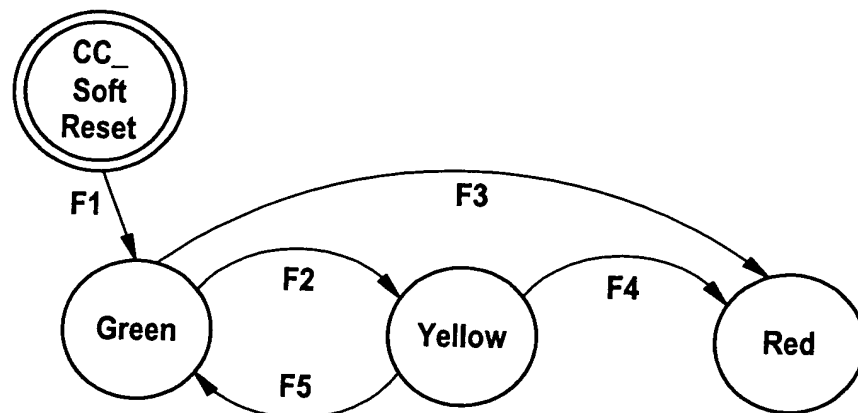


Fig. 73

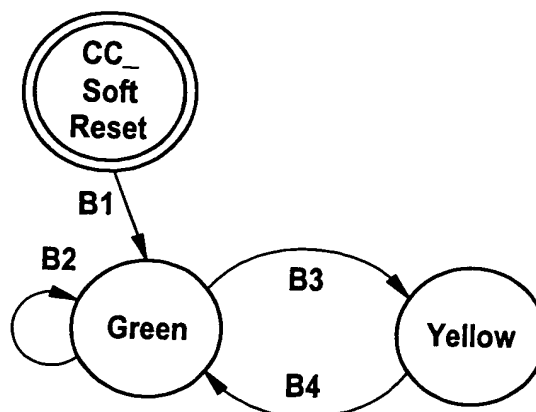


Fig. 74

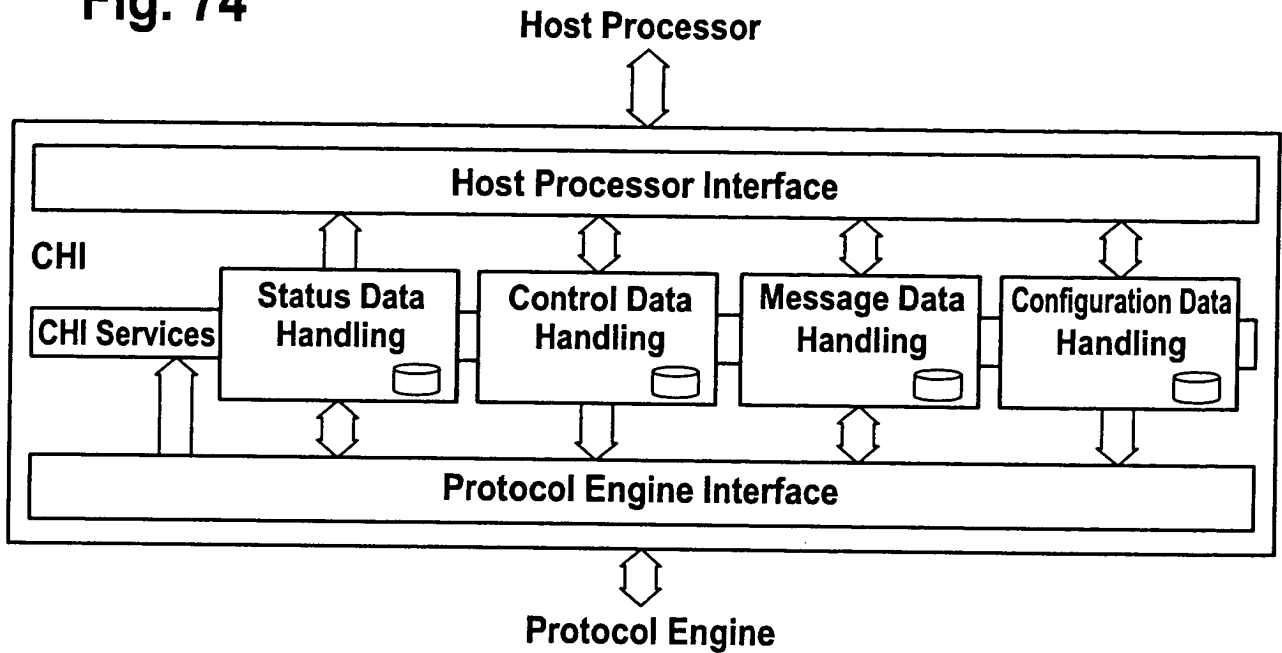


Fig. 75

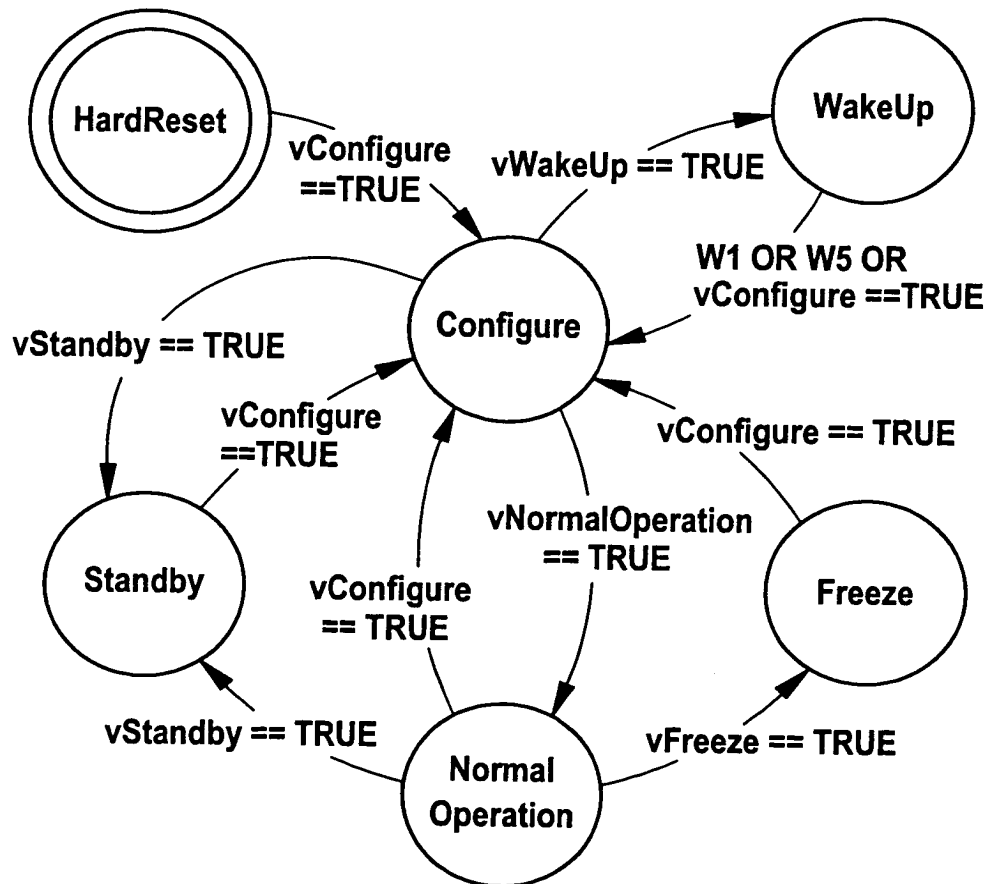


Fig. 76

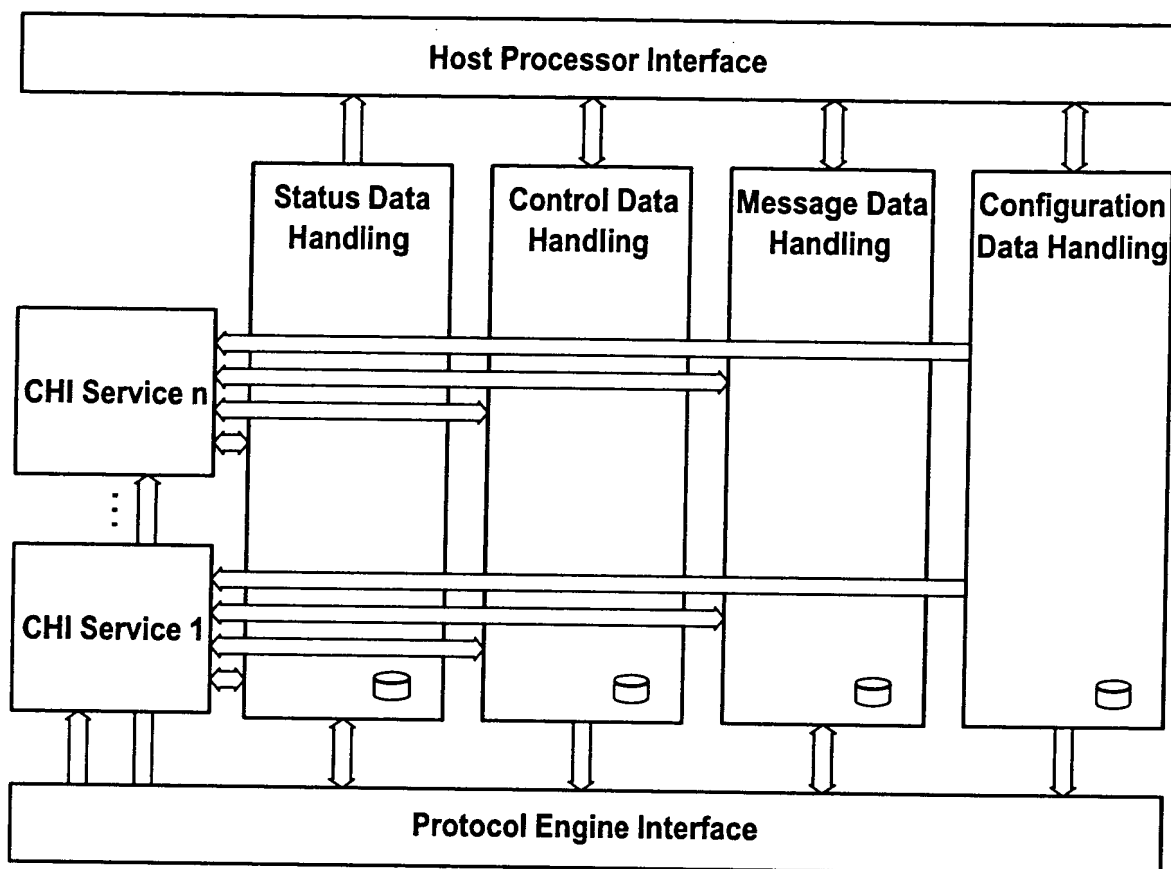


Fig. 77

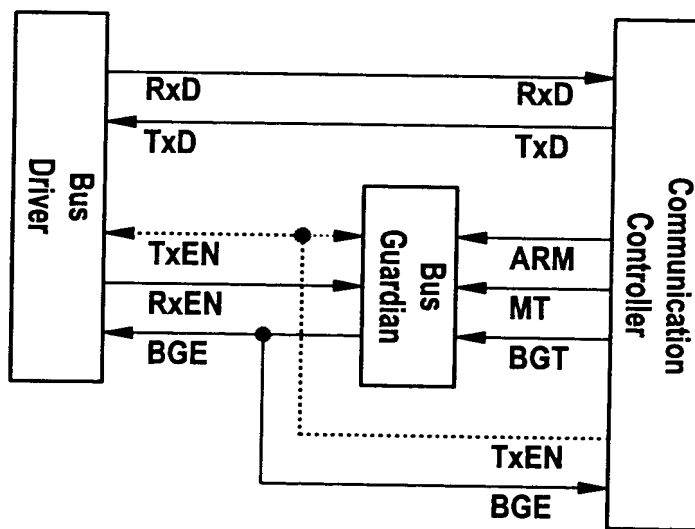


Fig. 78

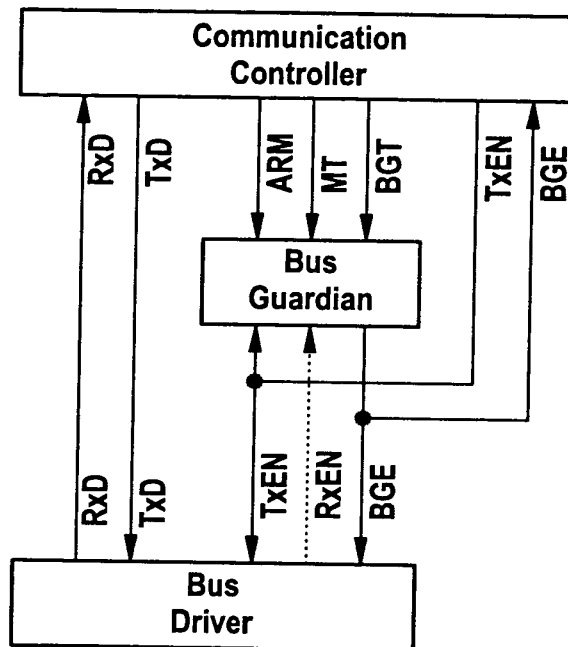


Fig. 79

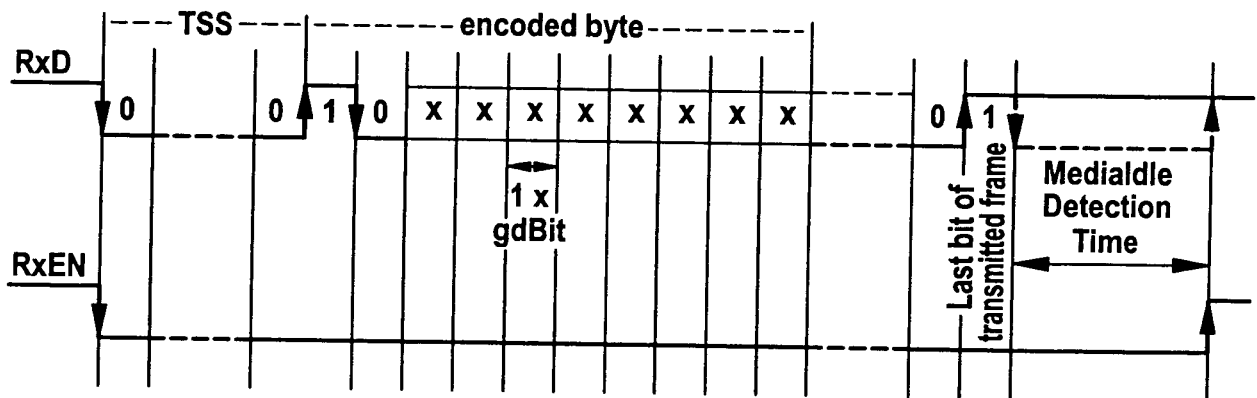


Fig. 80

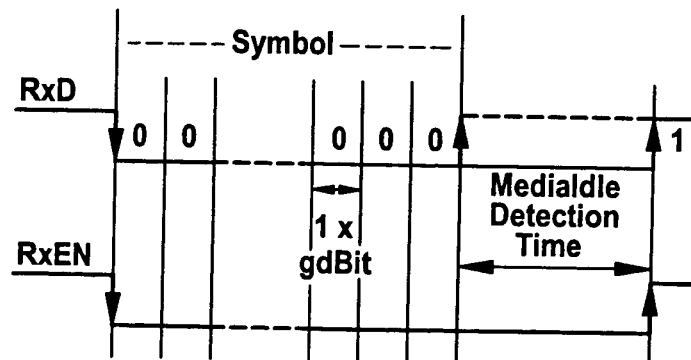


Fig. 81

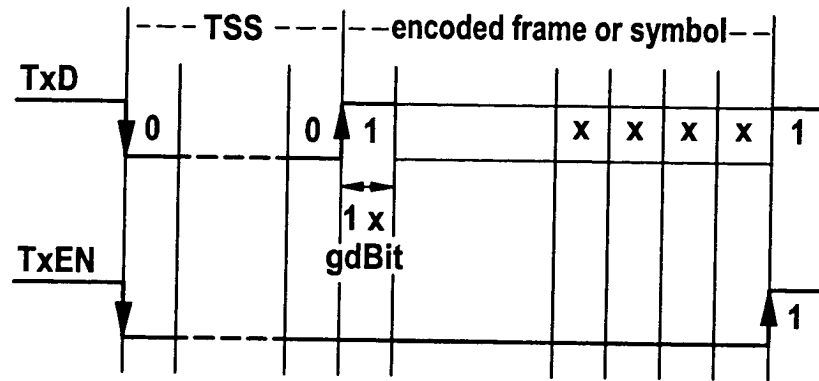


Fig. 82

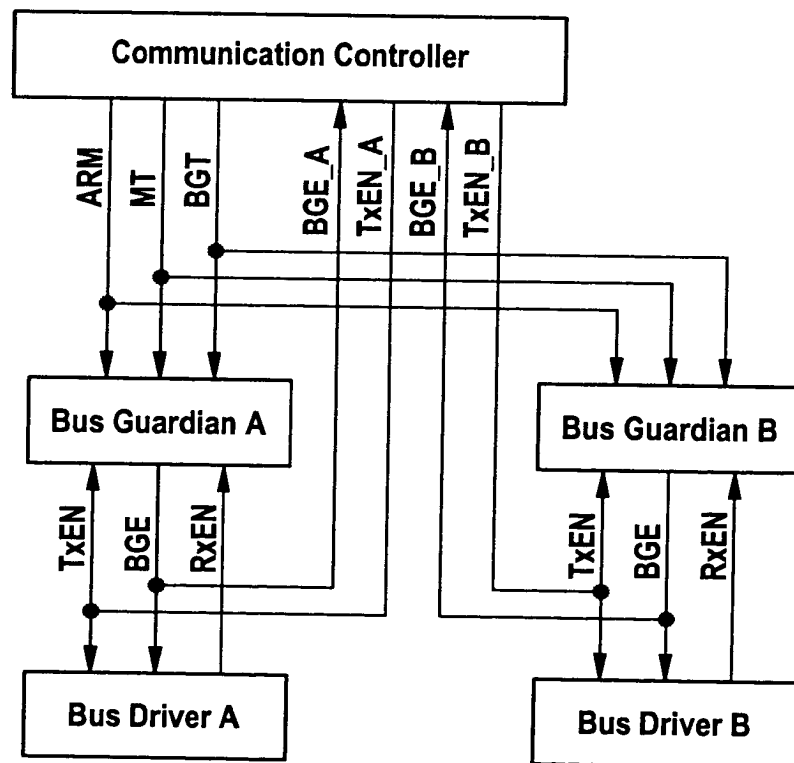


Fig. 83

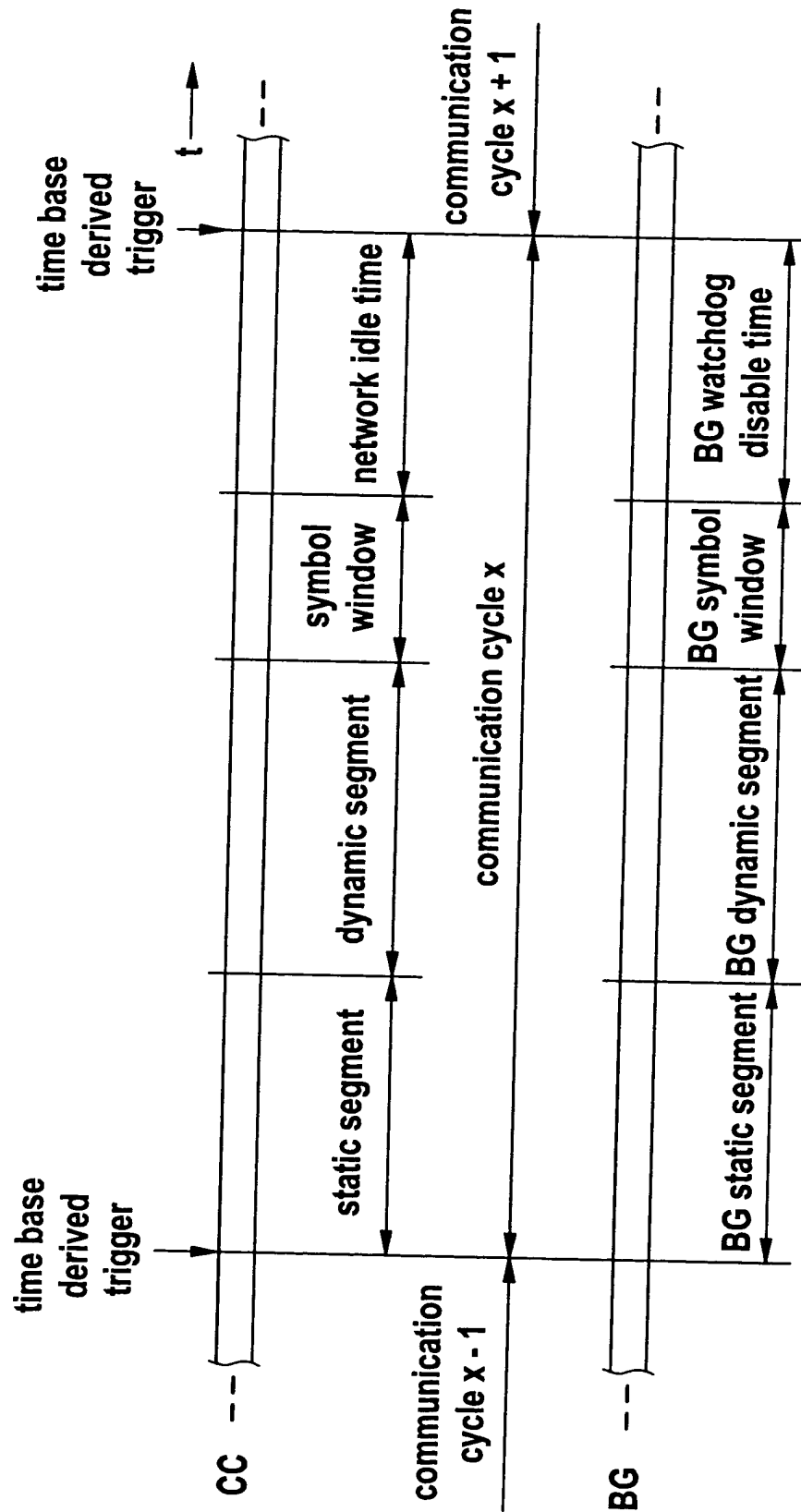


Fig. 84

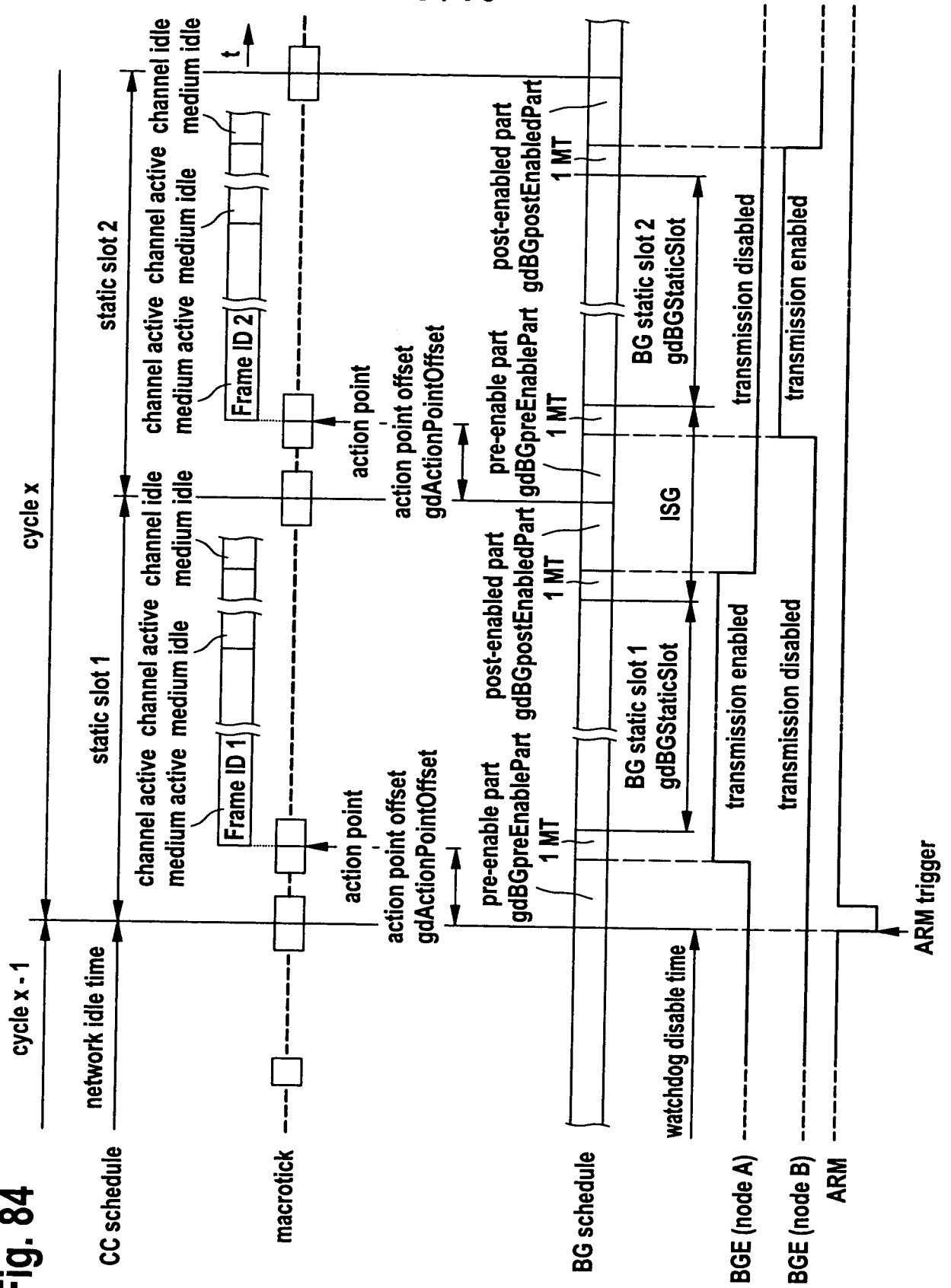


Fig. 85

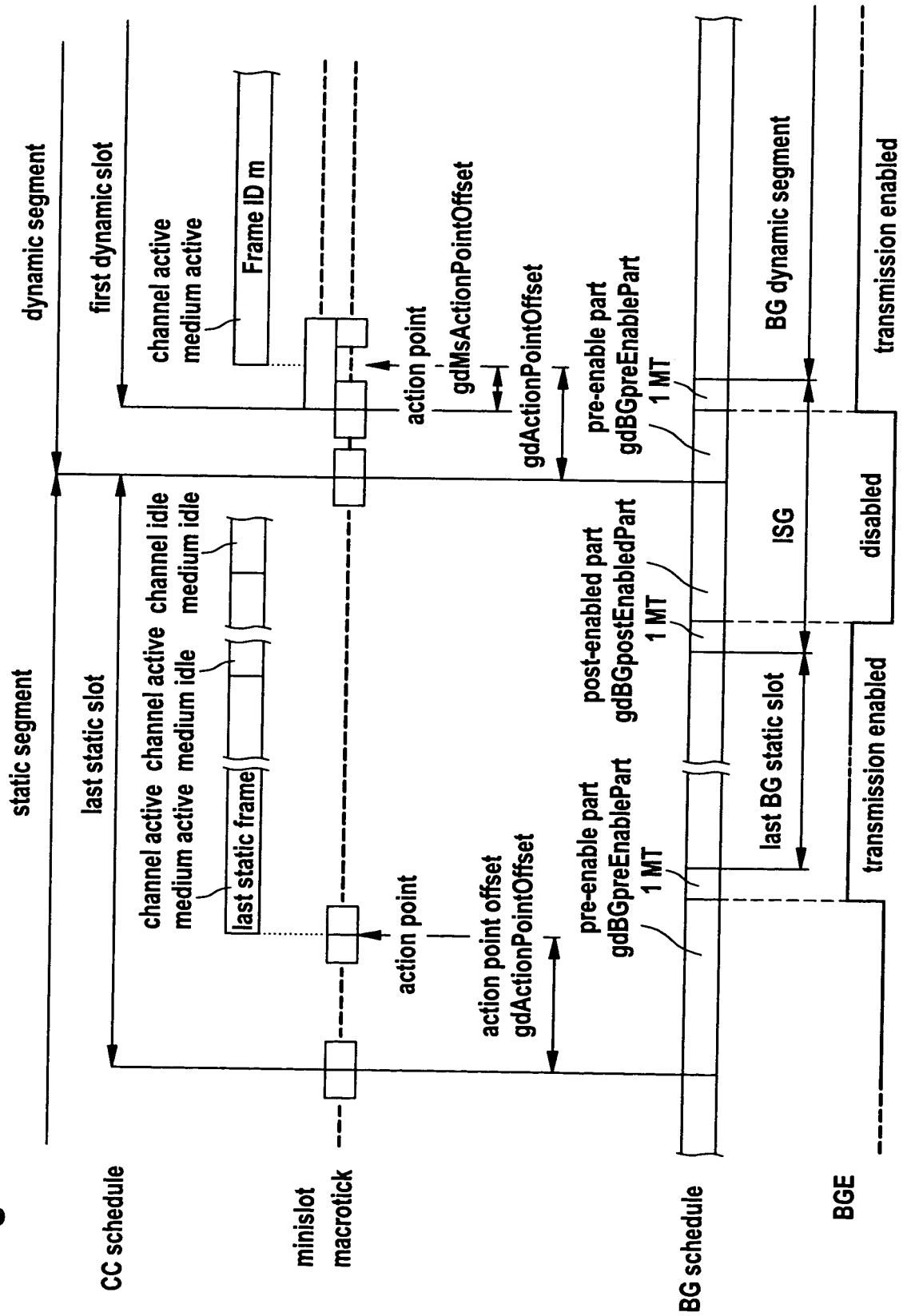
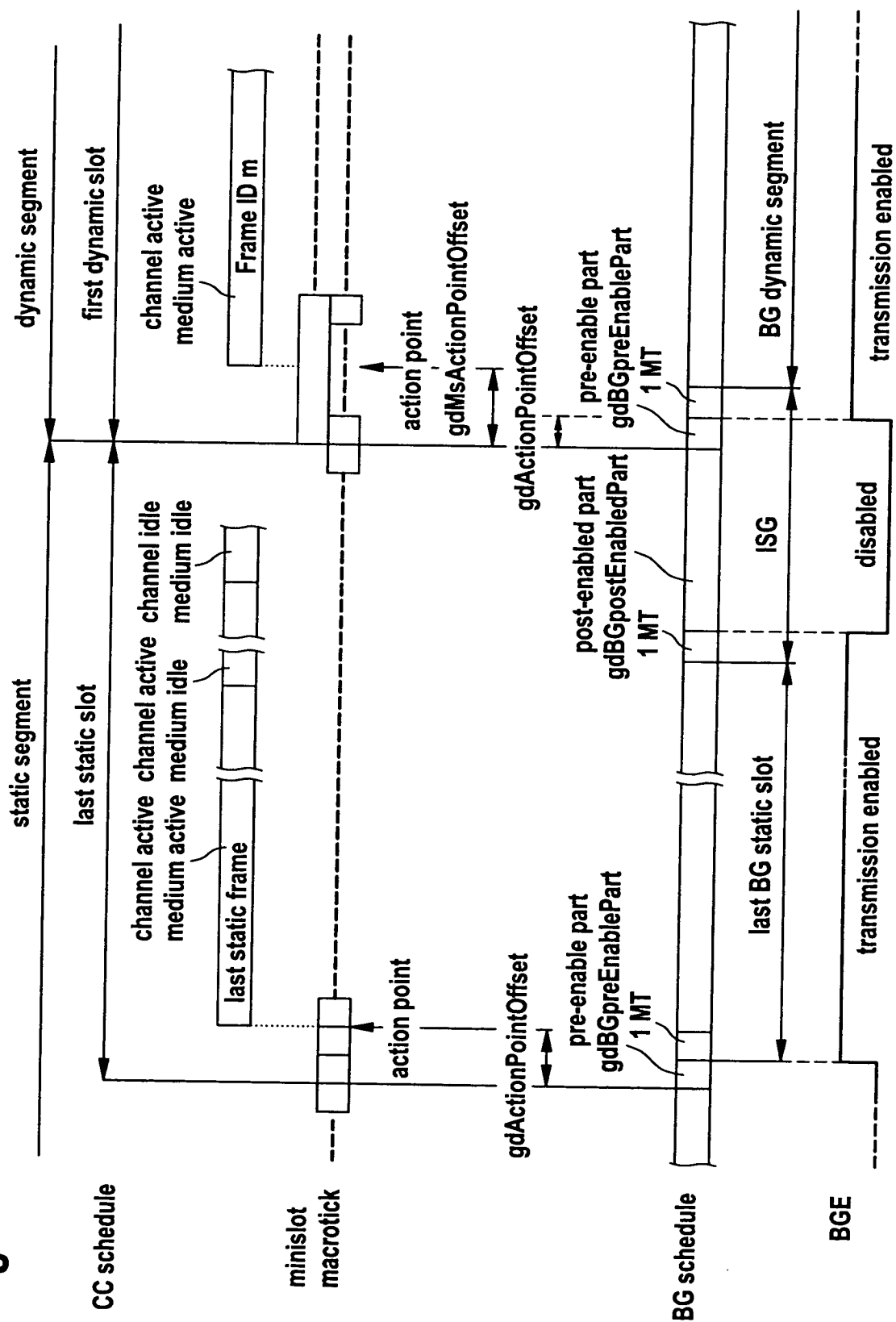


Fig. 86



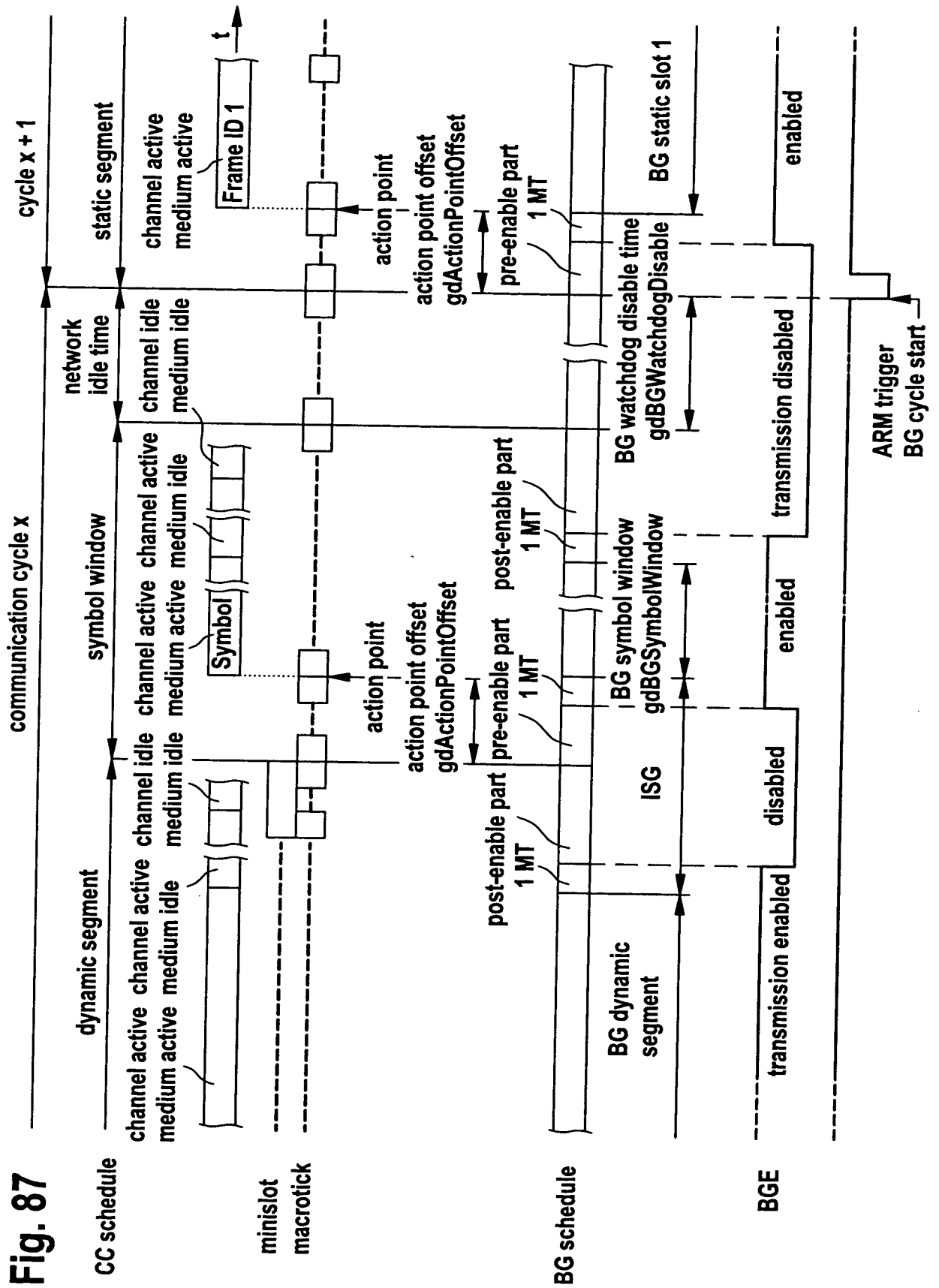


Fig. 88

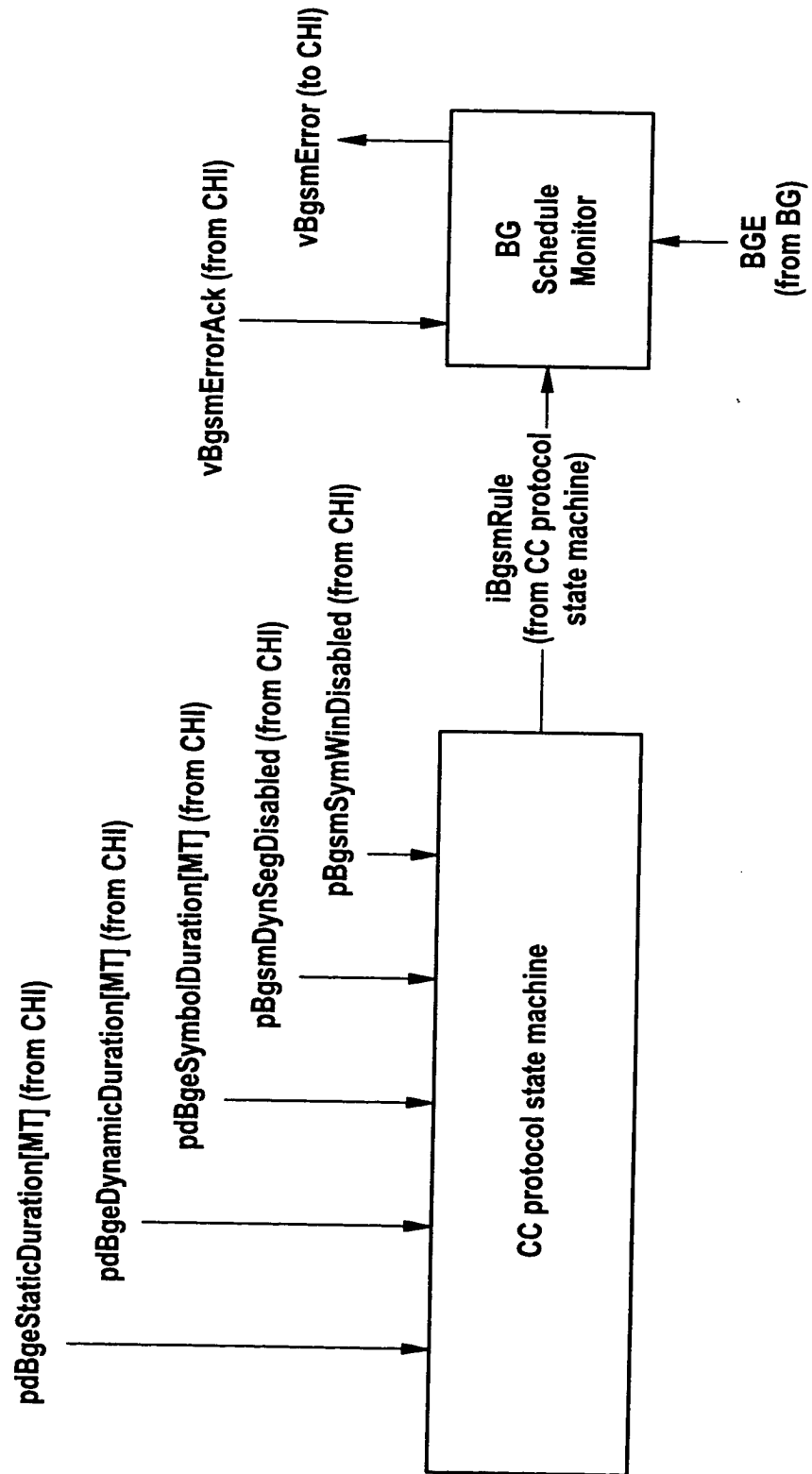


Fig. 89

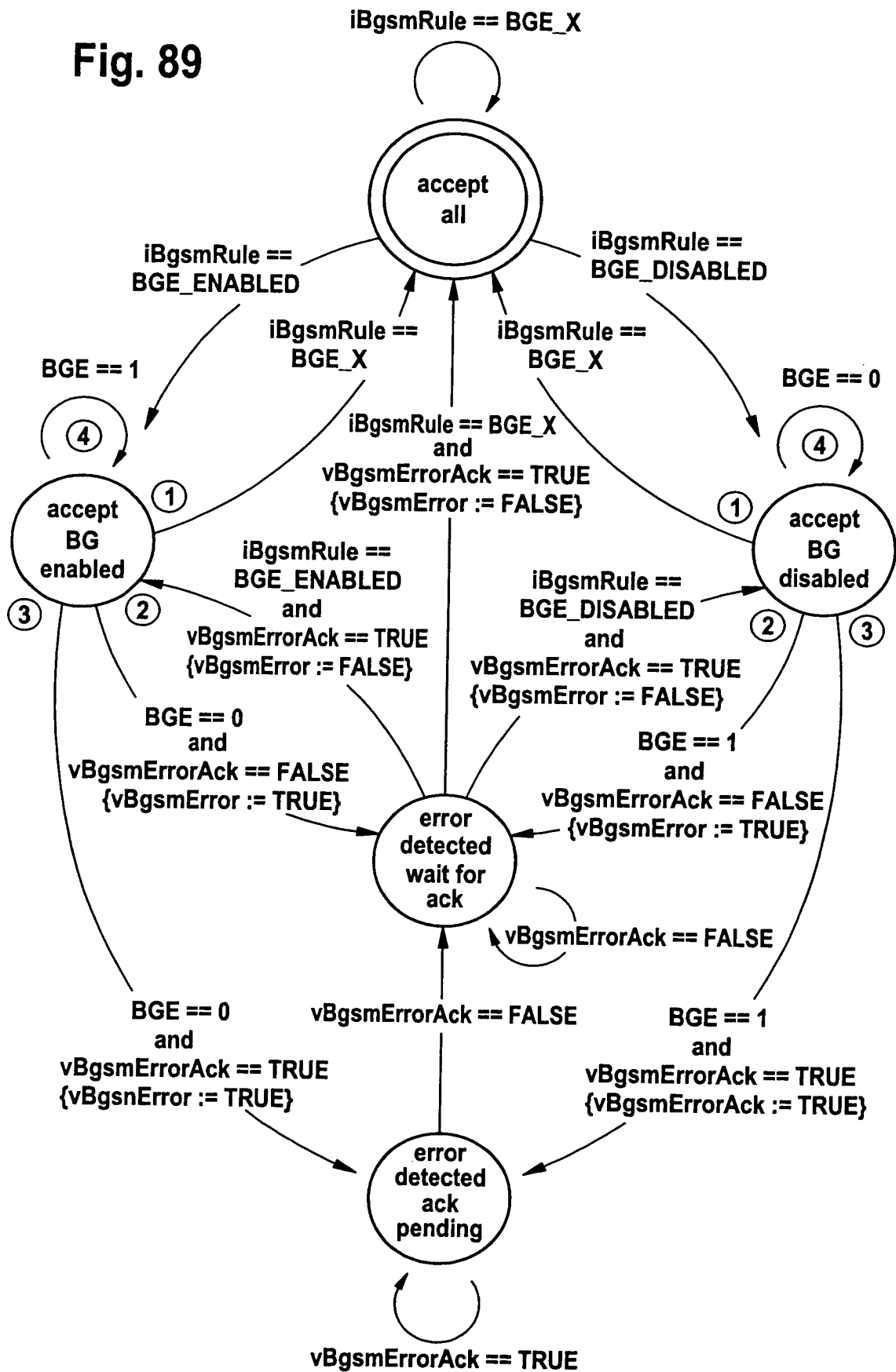
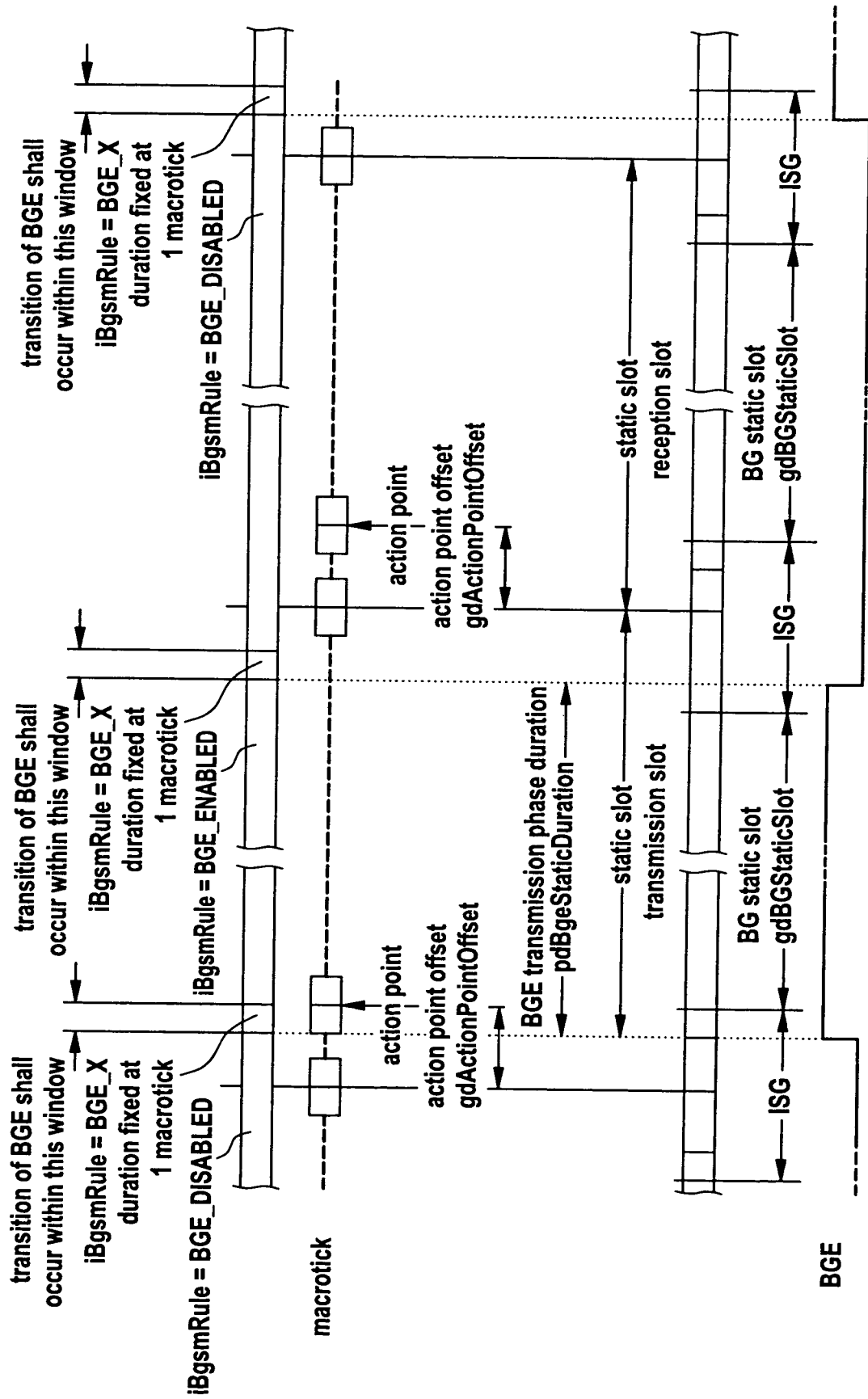


Fig. 90



The diagram illustrates the timing of BGE static slots and reception slots. It is divided into three main sections for static slots and one for reception slots.

Static Slot Timing:

- Transition Window:** The transition of BGE shall occur within this window. This window is defined by $iBgsRule = BGE_X$ and has a duration fixed at 1 macrotick.
- Action Point:** The action point is defined by the action point offset and the $gdActionPointOffset$.
- Static Slot:** The static slot is defined by the BGE transmission phase duration and the $pdBgeStaticDuration$.

Reception Slot Timing:

- Static Slot:** The static slot is defined by the BG static slot and the $gdBGSlot$.
- ISG:** The ISG (Inter-Slot Guard) is the period between the end of the static slot and the start of the next static slot.

The diagram also shows the macrotick and BGE timelines, with the BGE timeline starting at the action point offset.

Fig. 93

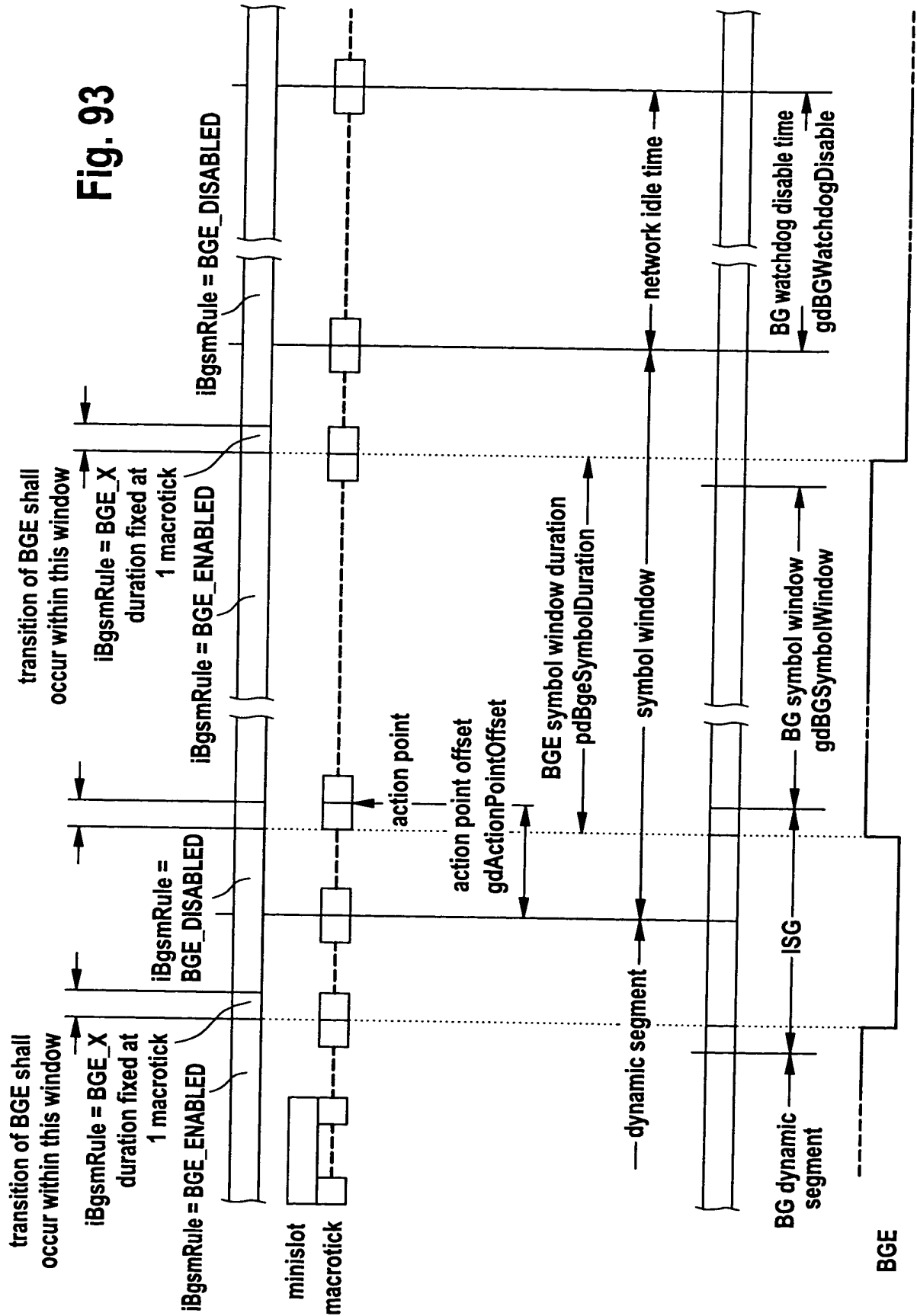


Fig. 94

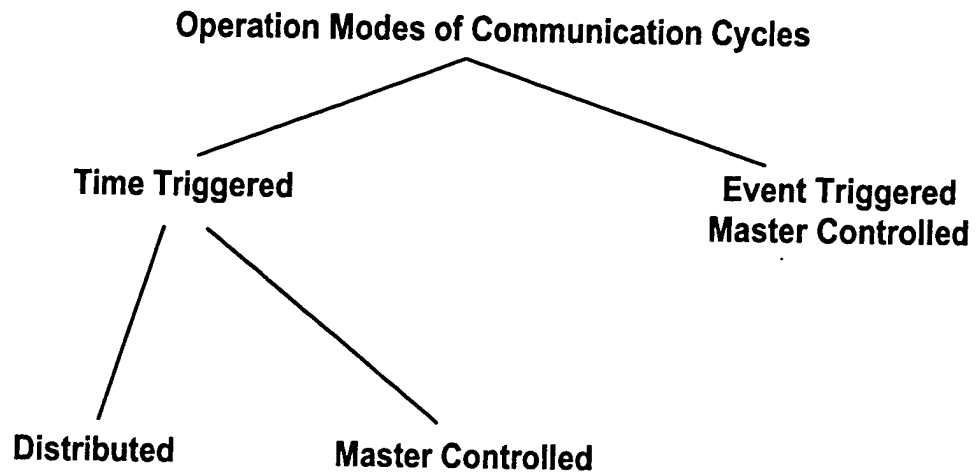


Fig. 95

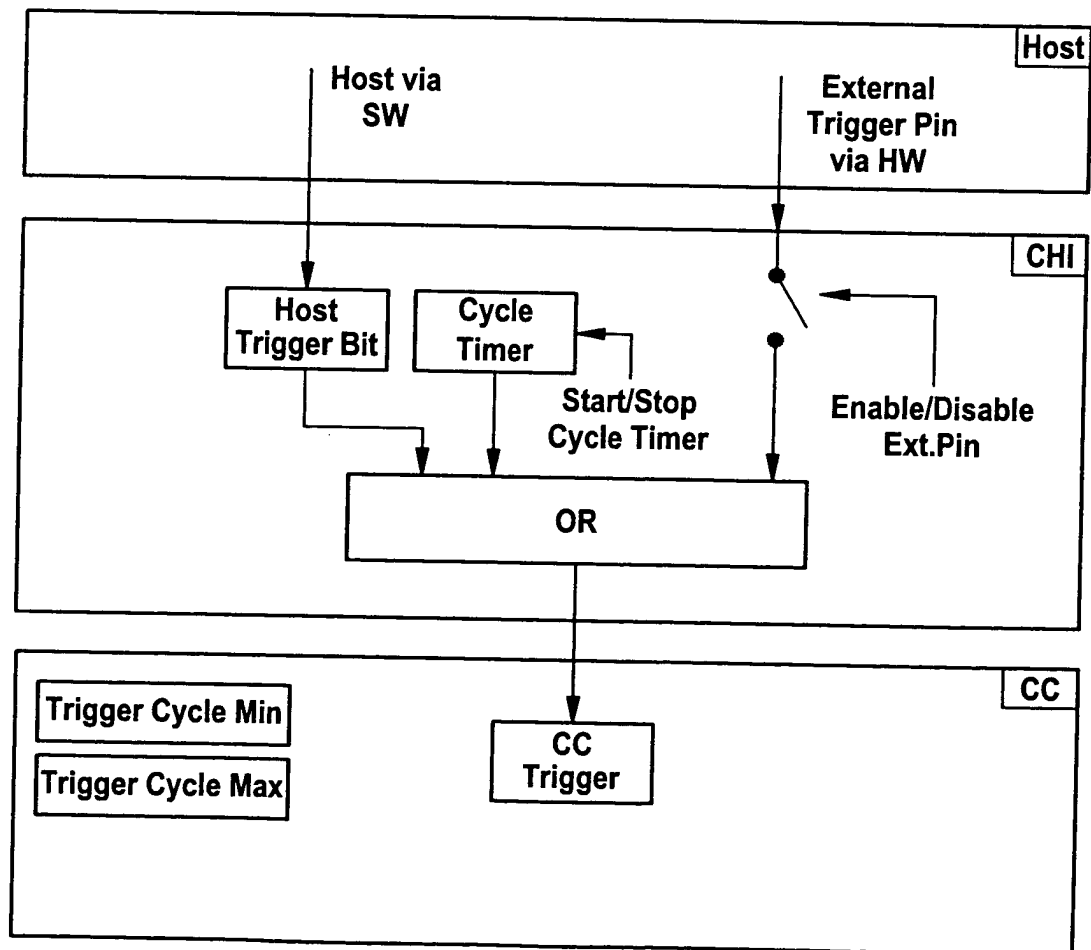


Fig. 96

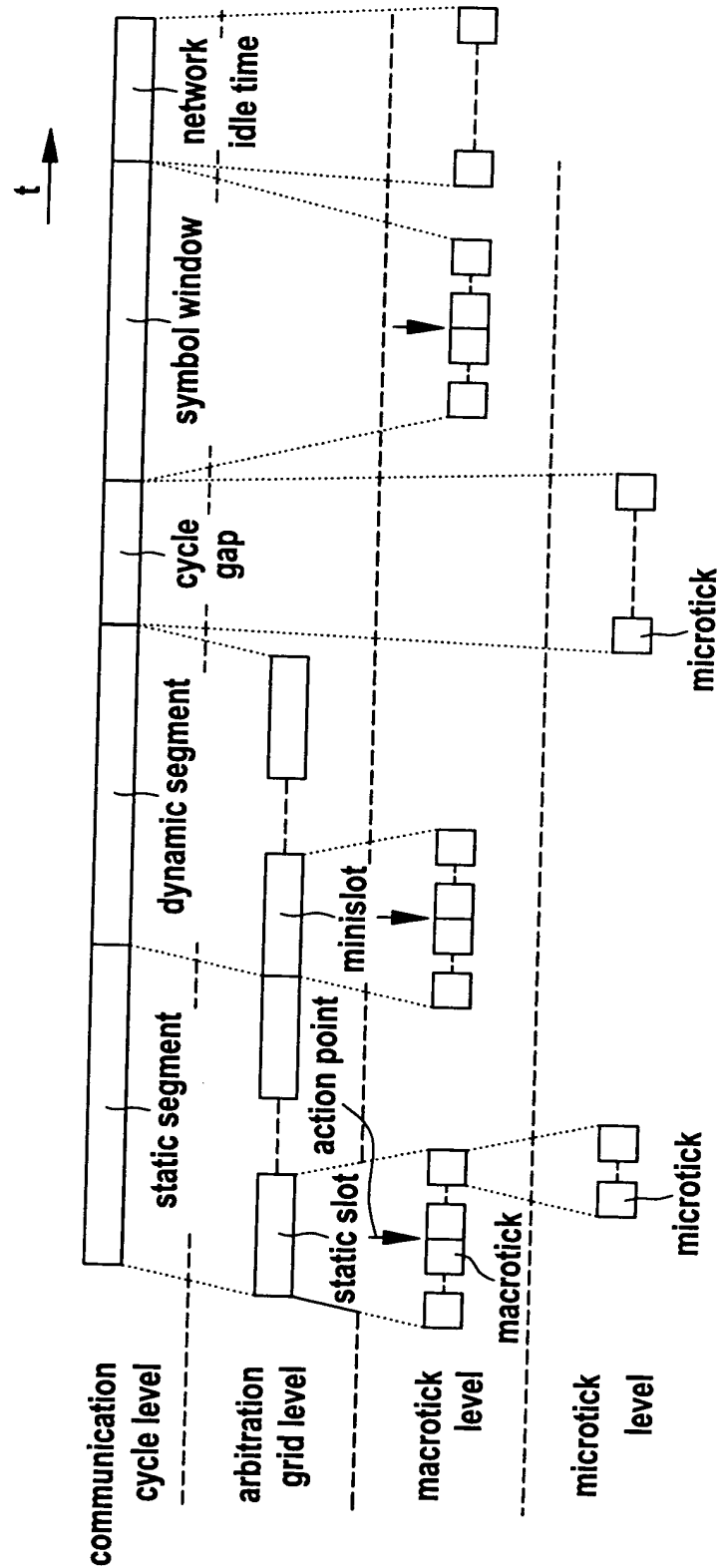


Fig. 97

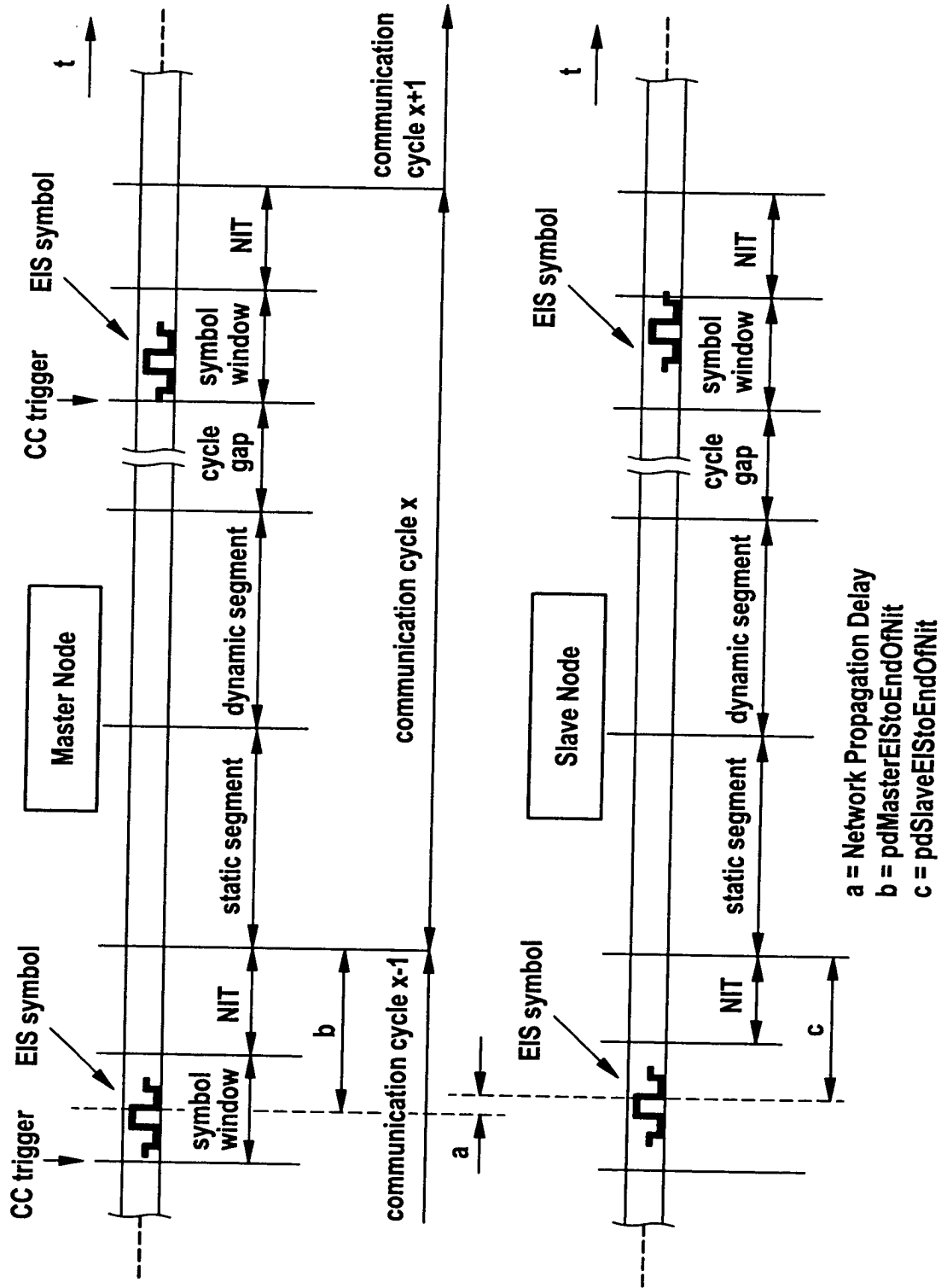


Fig. 98

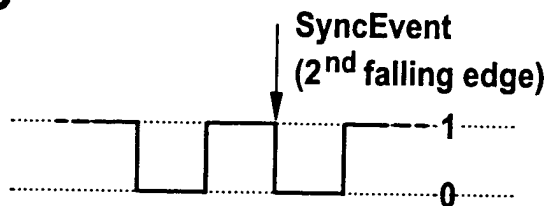


Fig. 99

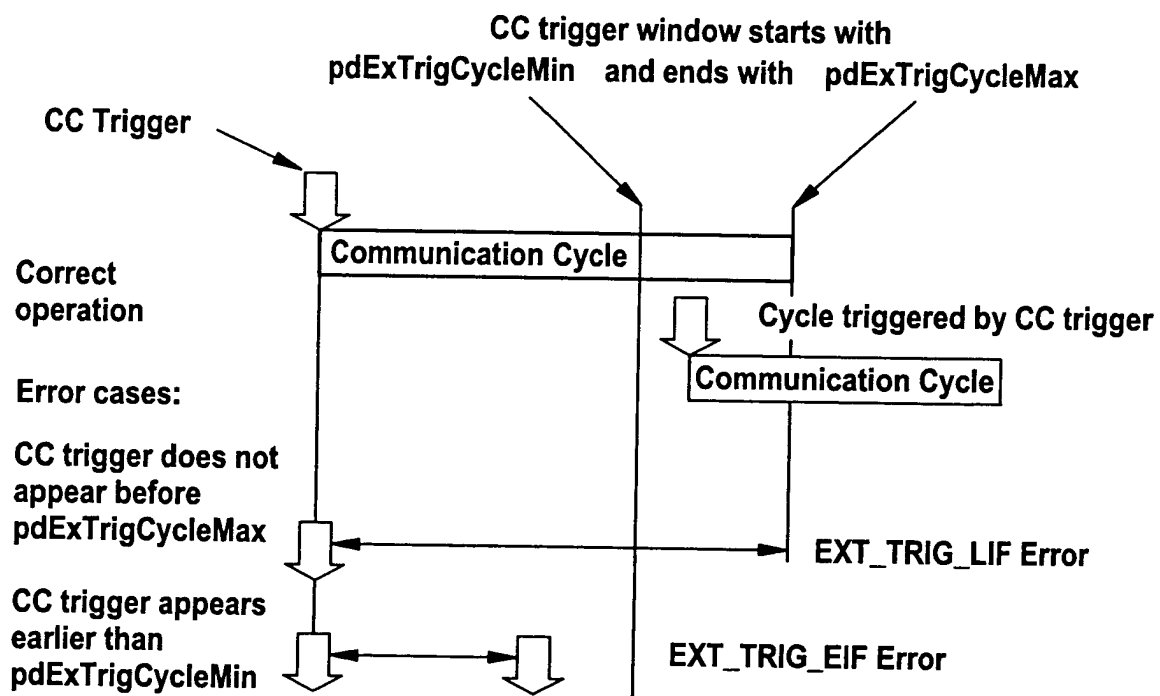


Fig. 100

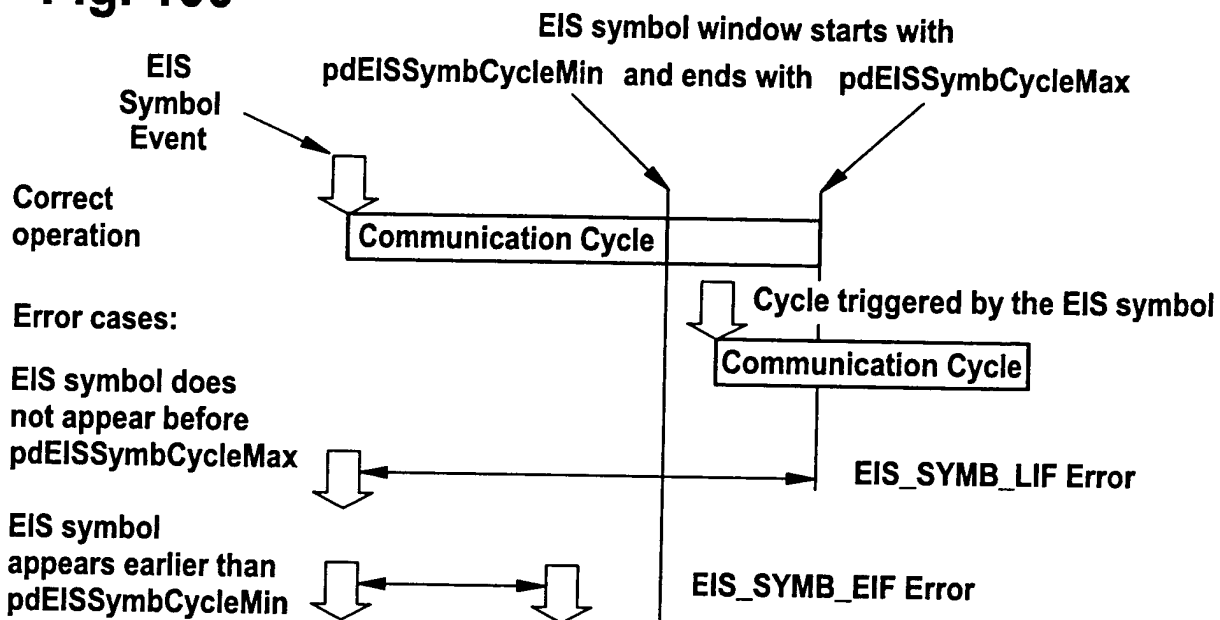


Fig. 101

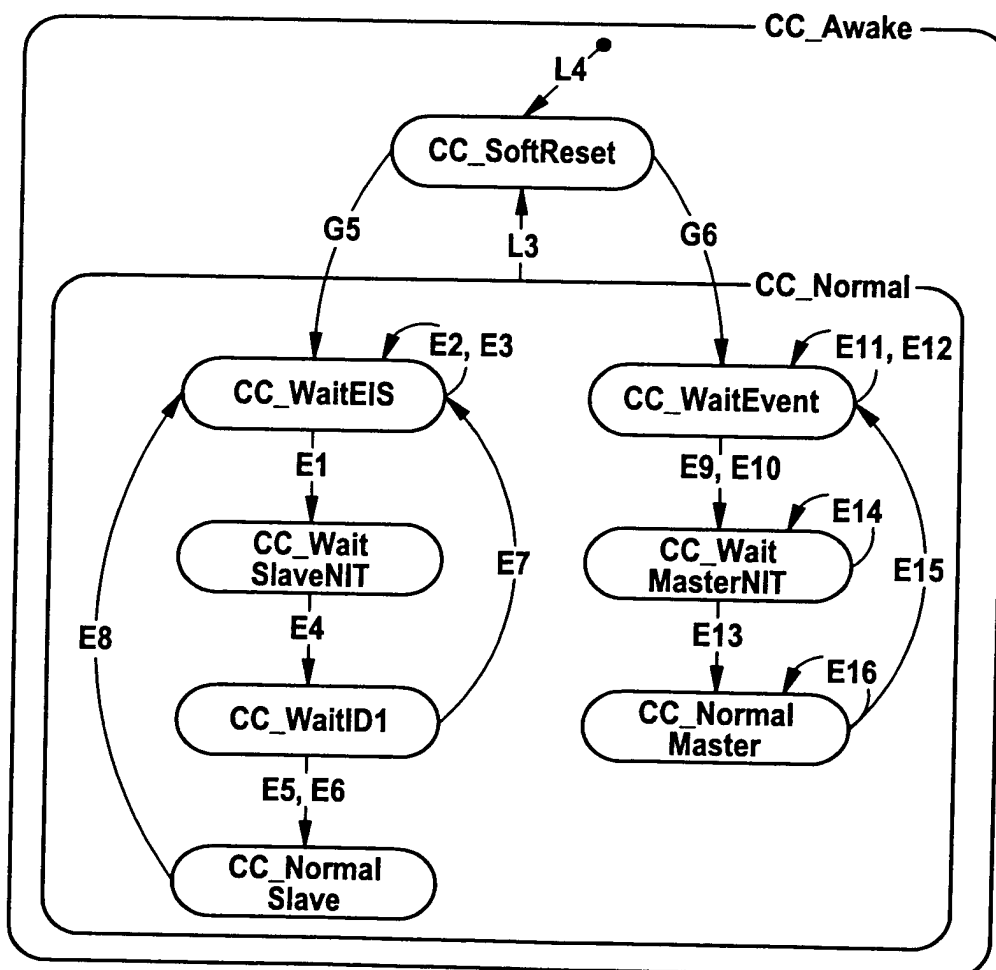


Fig. 102

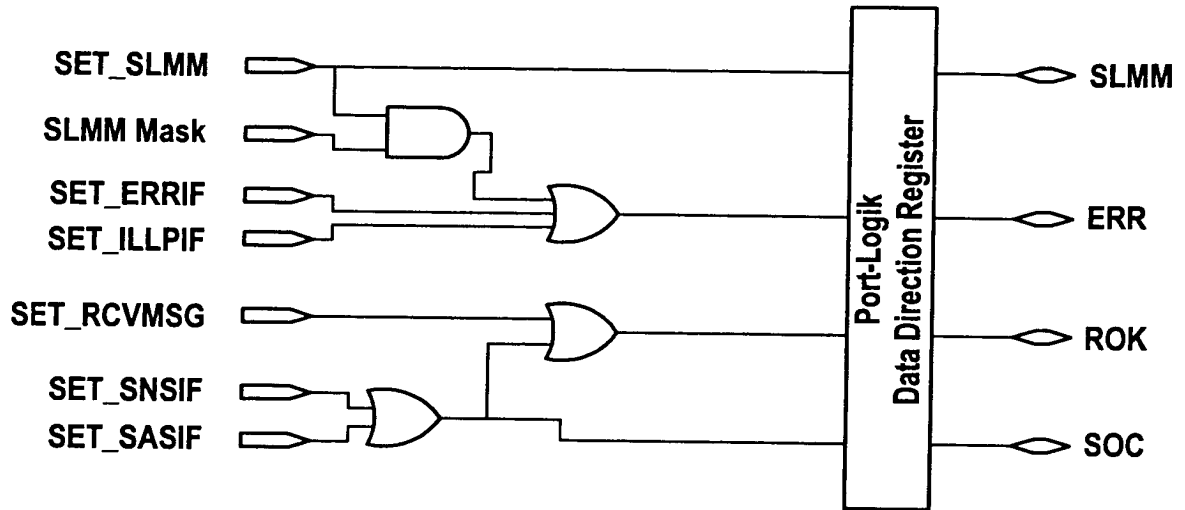


Fig. 103

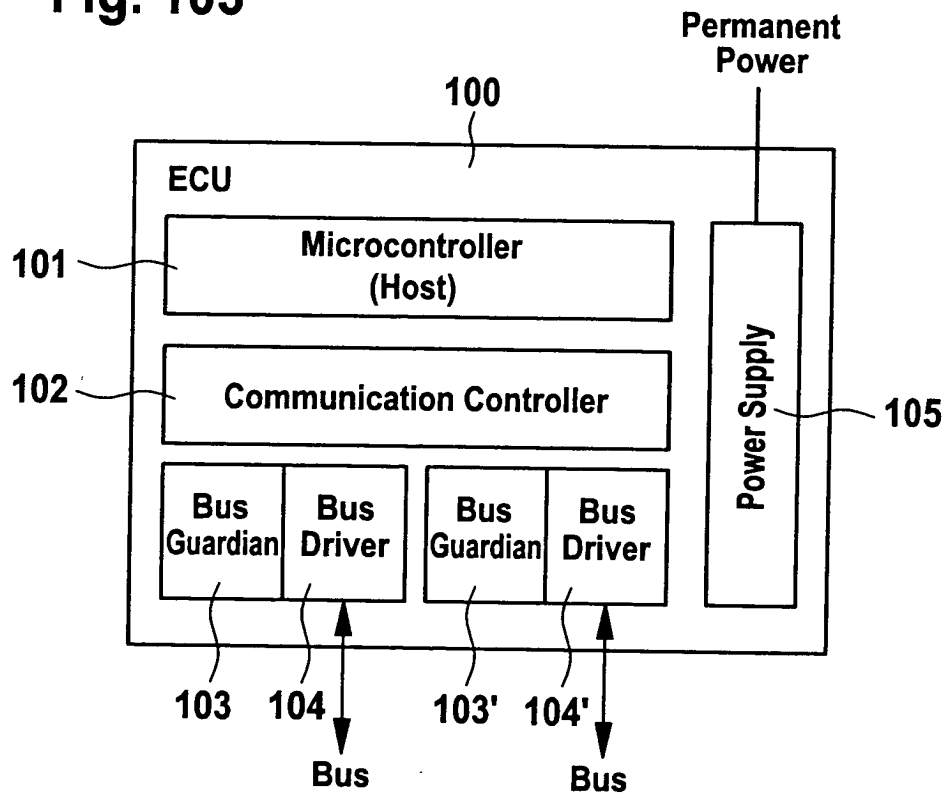


Fig. 104

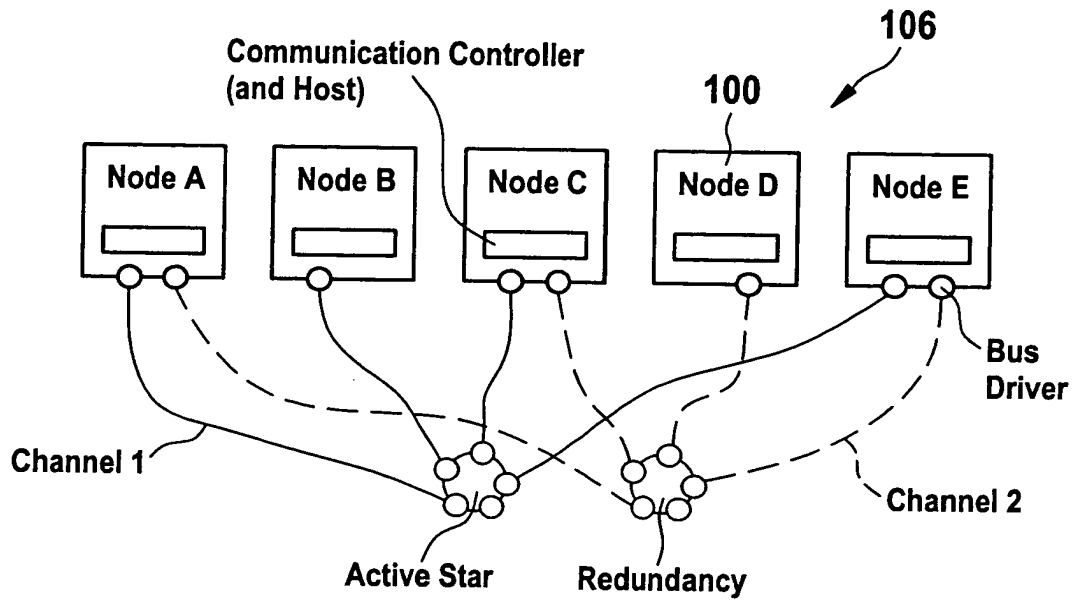


Fig. 105

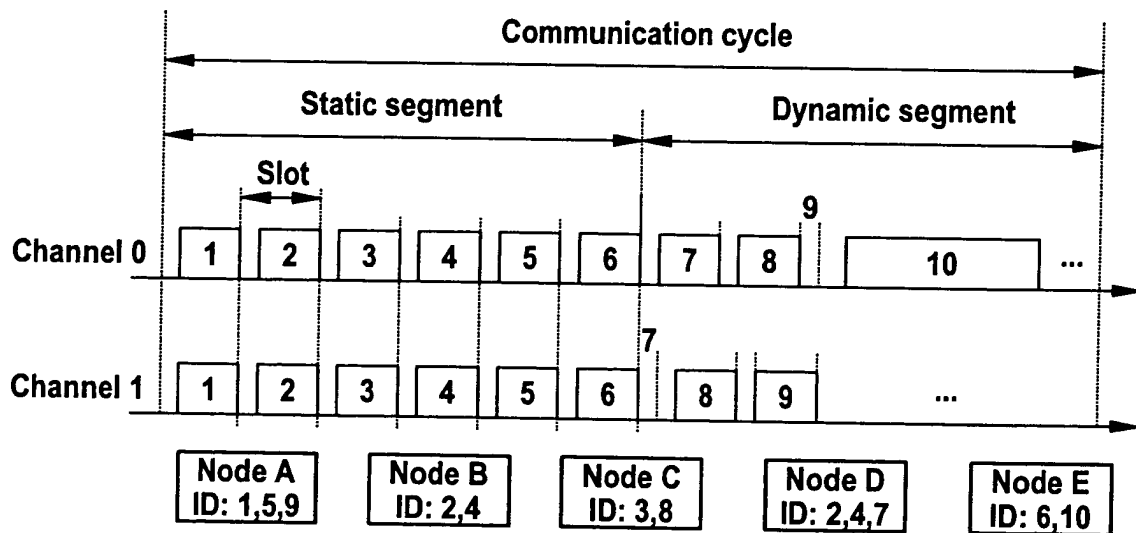


Fig. 106

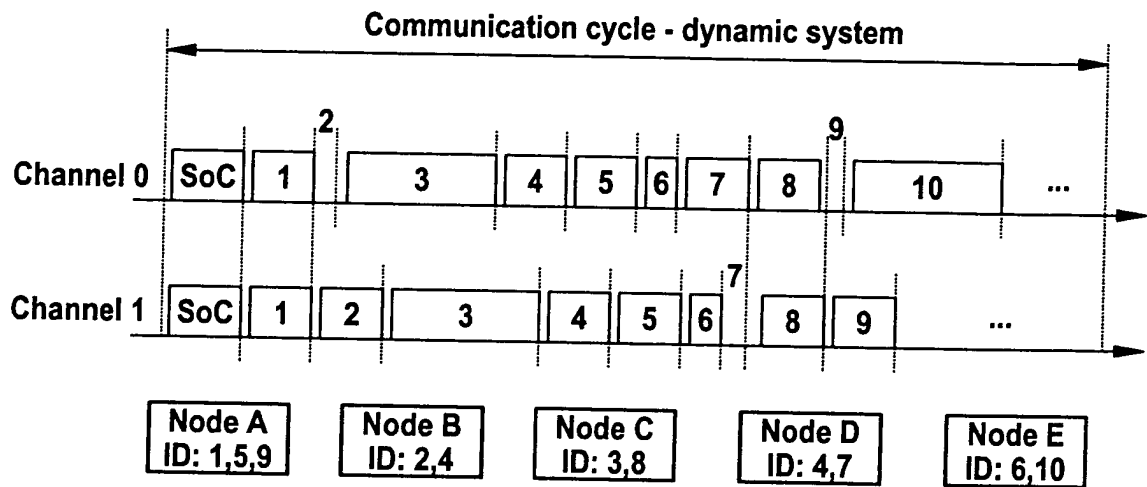


Fig. 107

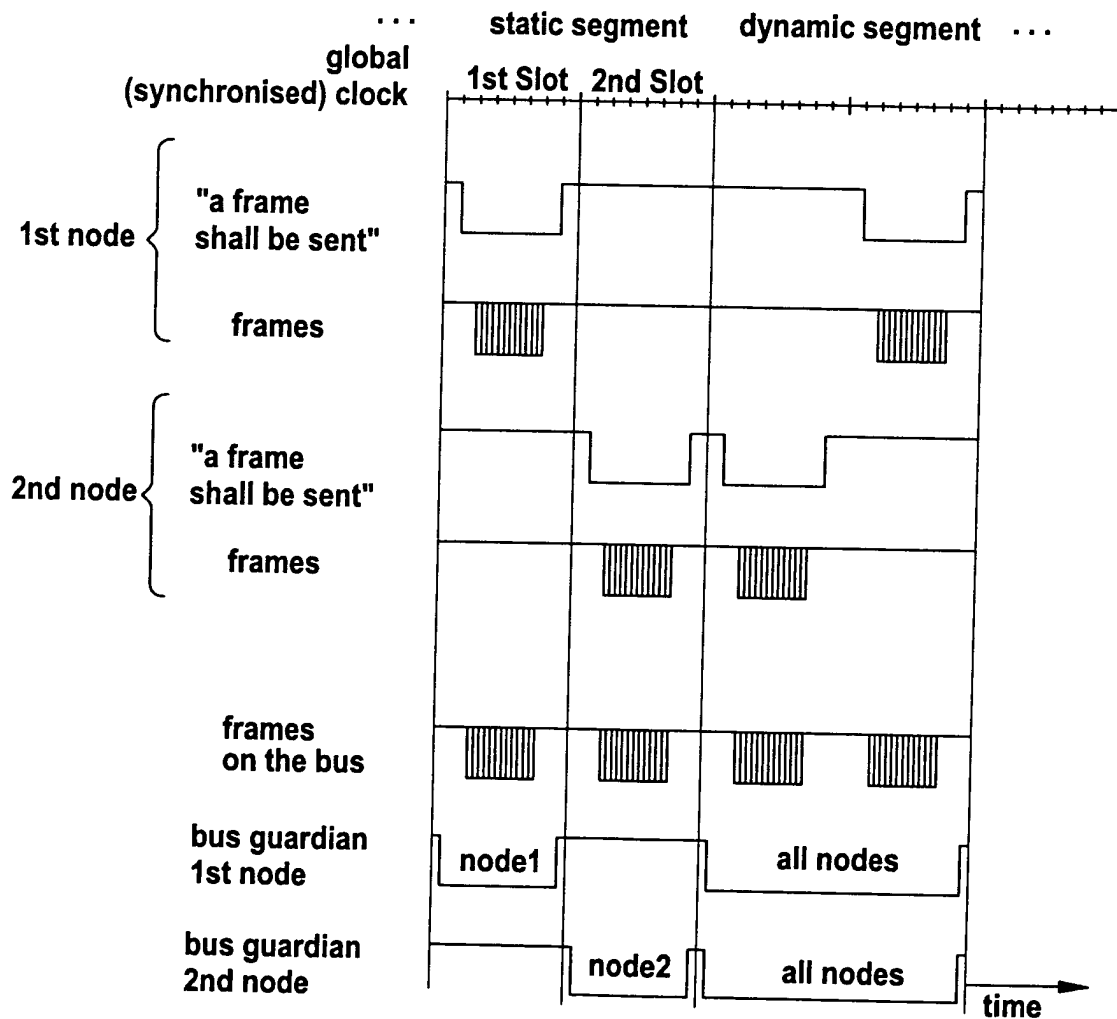


Fig. 108

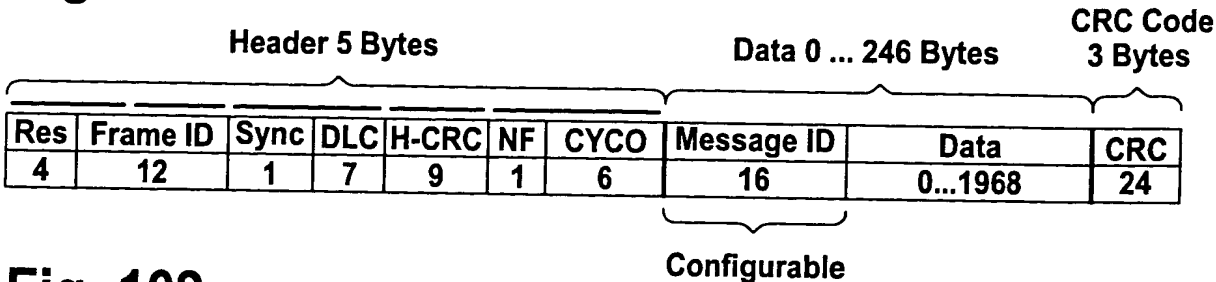


Fig. 109

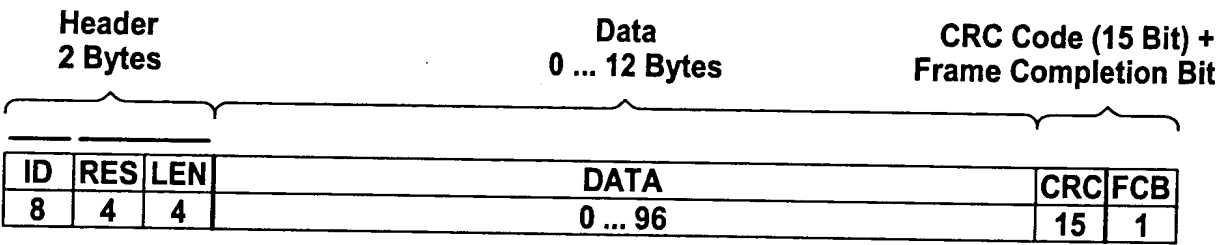


Fig. 110

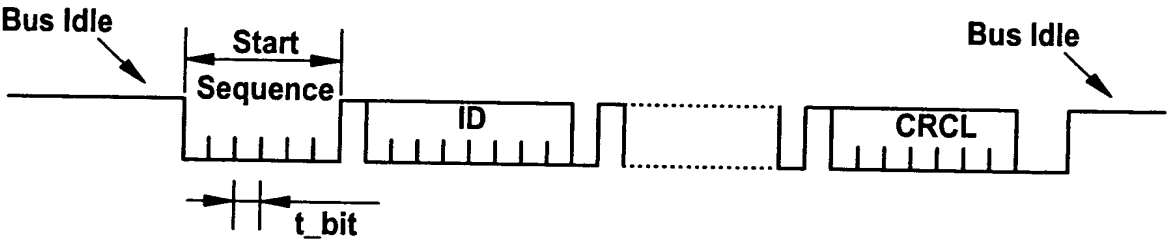


Fig. 111

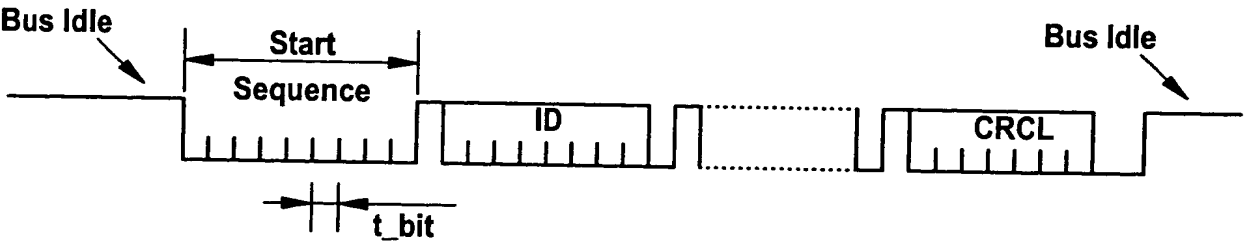


Fig. 112

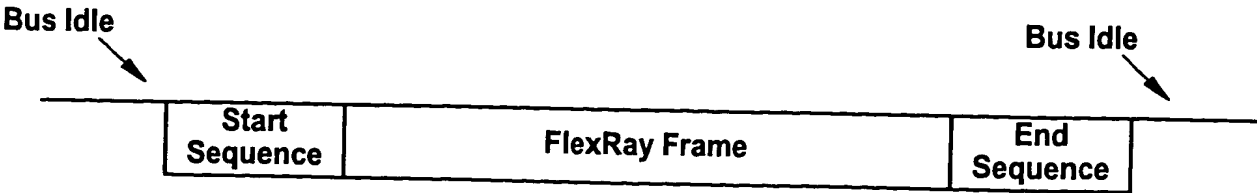


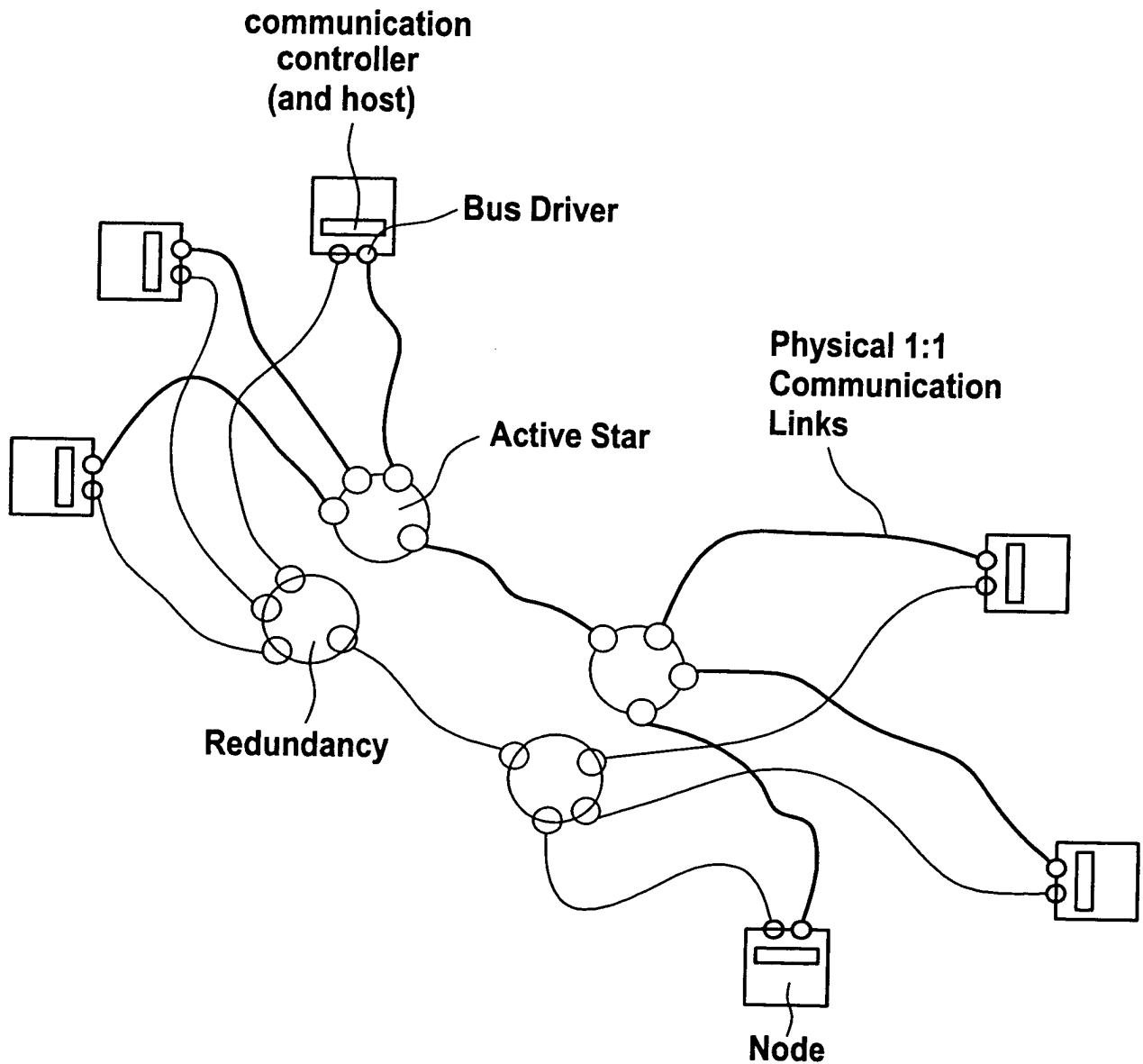
Fig. 113

Fig. 114

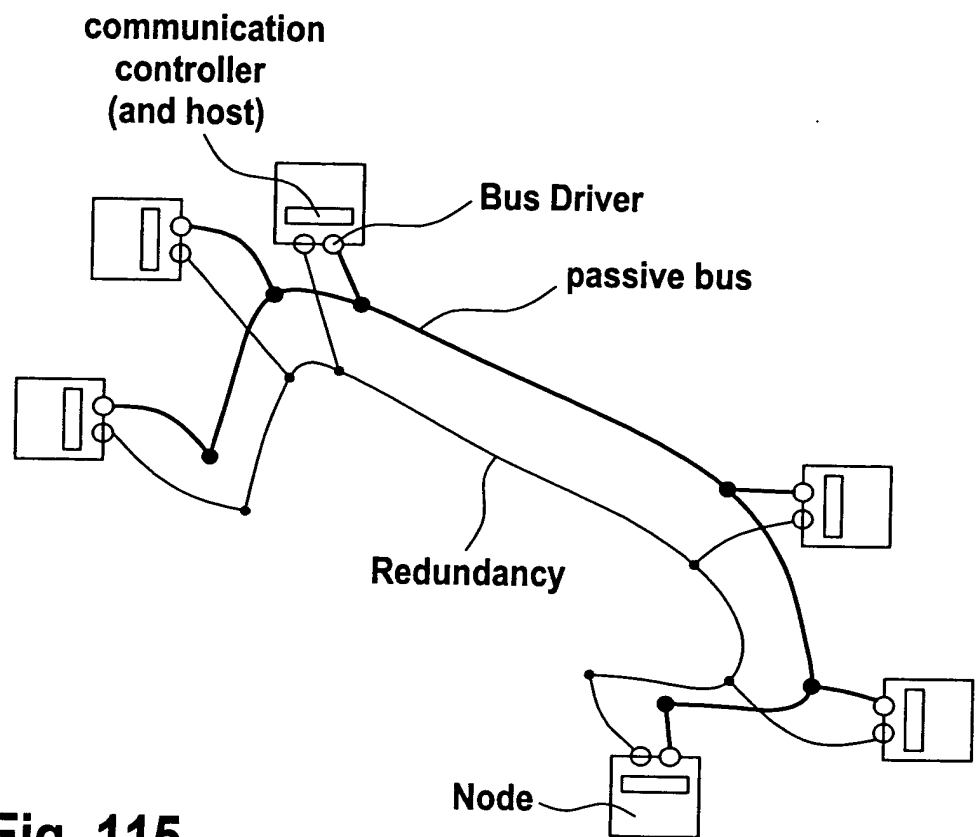


Fig. 115

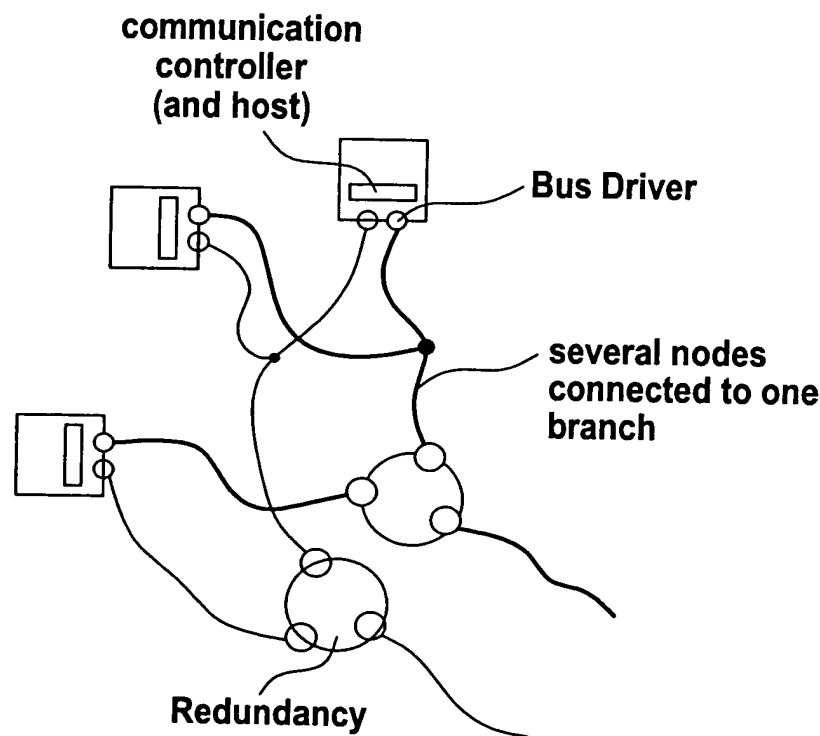


Fig. 116

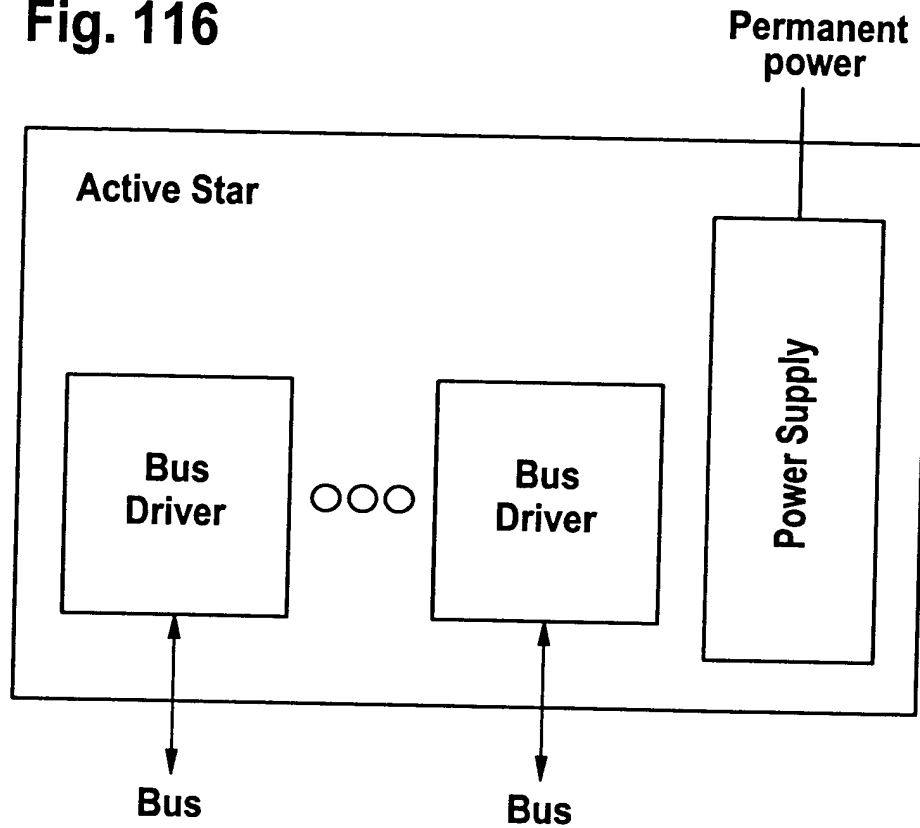


Fig. 117

